TERADYNE Z1800-Series

Component Test Reference

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PREFACE

This document is an alphabetical reference of analog and digital device tests. It starts with an explanation of shorthand and longhand test methods.

The analog component chapters cover shorthand and longhand test methods, test types, range and accuracy specifications, calculating test accuracy, and test step editing.

The digital section covers test techniques for SSI/MSI, non-programmable LSI, ROM and RAM devices, and ASICs and PALs, with the following subject areas:

- Test Philosophy
- Test Specifications
- Gray-Code Test Methods
- Vector Test Methods
- Digital Test Editing

Refer to the **Z1800-Series Programmer's Guidebook**, Chapter 12, for vector test strategies.

The table below describes the unit multipliers or scales that appear often in this reference and throughout the software.

Multiplier	Unit	Example	X Multiplier
U (micro)	V (Volt)	UV	10^{-6}
M (milli)	V (Volt)	MV	10^{-3}
K (kilo)	O (Ohm)	KO	10^{3}
M (mega)	O (Ohm)	MO	10^{6}
N (nano)	A (Ampere)	NA	10^{-9}
U (micro)	A (Ampere)	UA	10^{-6}
M (milli)	A (Ampere)	MA	10^{-3}
U (micro)	H (Henry)	UH	10^{-6}
M (milli)	H (Henry)	MH	10^{-3}
P (pico)	F (Farad)	PF	10^{-12}
N (nano)	F (Farad)	NF	10^{-9}
U (micro)	F (Farad)	UF	10^{-6}
M (milli)	F (Farad)	MF	10^{-3}
M (milli)	S (seconds)	MS	10^{-3}

1 SHORTHAND AND LONGHAND TESTING

The test system can take analog measurements in two distinct modes: shorthand and longhand.

Common to both shorthand and longhand tests is the ability to apply six decimal precision to test limits such as Value, High and Low. When you select Scale in the worksheet, a pop-up menu appears where you select the scale and either **Default** or **6 decimal** precision. All existing programs have Default selected, which is the backwards compatible mode. In Default, values greater than or equal to 100.0 have two decimal precision; all other values have three decimal precision.

PRISM-Z

The PRISM-Z (PRecision Integrated Signal Measurement) module is a next generation analog measurement subsystem for in-circuit testers. It is a Digital Signal Processor-based (DSP) design that accurately measures values and circuit configuration. The PRISM-Z instrument is an option for Z1800-Series systems.

Systems that include the PRISM-Z option retain the ATB (Analog Test Board) in order to guarantee backward compatibility with existing programs as well as for ordinary tasks such as shorts, continuities, and Node Finder. You can mix and match PRISM-Z and ATB tests throughout your test program. The following test types are available on F.2a and later versions of 18xx system software:

- Capacitor
- Inductor
- Resistor
- Test I Stim V
- Test V
- Test V Stim I
- Test V Stim V

You can convert existing component tests that use ATB worksheets to tests that use PRISM-Z worksheets. You can also convert PRISM-Z worksheets back to ATB.

Refer to the **Z1800-Series PRISM-Z User's Guide** for a complete discussion about the PRISM-Z test types available for longhand and shorthand tests.

Shorthand Tests

Shorthand test modes are geared toward specific component tests. In such tests, parameters are expressed in the components' native units (i.e., Ohms for resistors), and compensation is automatically made for parasitic system components and errors before a result is displayed and compared to the test limits.

Refer to specific components, such as Capacitor, Resistor, Transistor, for information about shorthand testing.

Longhand Tests

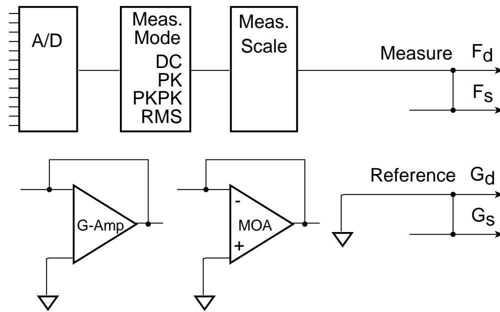
Longhand tests, on the other hand, are more generic. Parameters must be expressed in generic units of volts and amperes, and parasitic system components are not compensated for. While the shorthand test mode is simple to use, longhand gives more control over the features of the ATB. However, the longhand mode makes programming more complex and is prone to yielding erroneous results. For success in longhand tests, you need to have a solid understanding of operation-amplifier theory.

Longhand tests are grouped into four categories:

- Test V
- Test V Stim V, Test V Stim V Stim V
- Test V Stim I, Test V Stim I Stim V
- Test I Stim V, Test I Stim V Stim V

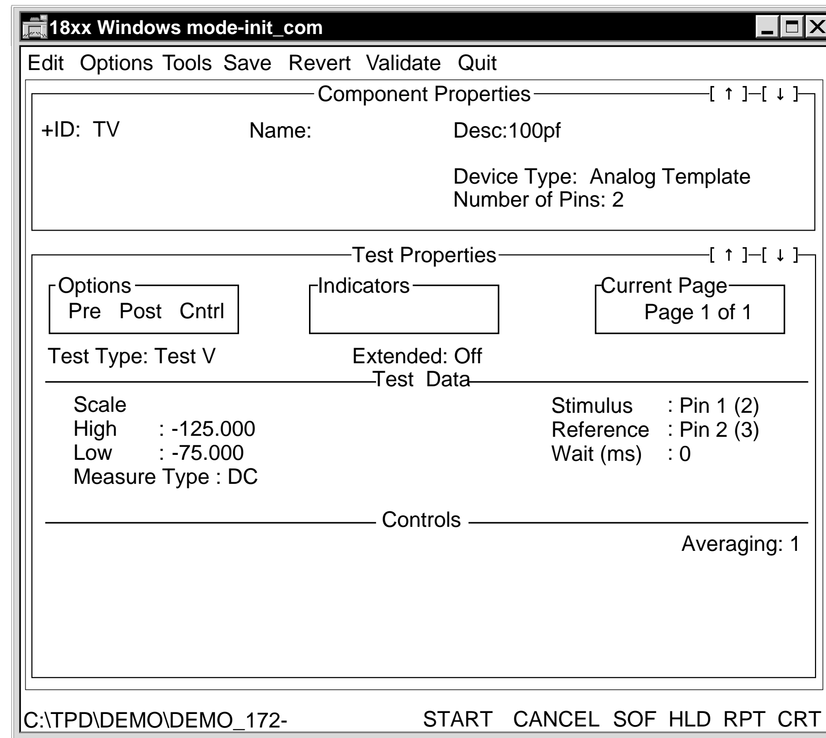
Test V

Test V mode sets the ATB up for basic voltage measurements according the following diagram.



The Worksheet

The following illustration shows the work sheet for Test.



Test Data for Test V /Test Properties Portion of Step Worksheet

Test V Type:

Scale	Measurement-related modifier—uv, mv, V
High	Upper limit for a passing measurement. Range = -1000 to +1000
Low	Lower limit for a passing measurement. Range =-1000 to +1000
Measure Type	DC, Peak, RMS, or Pk-Pk (peak to peak)
Measure	Pin/node number(s) at which measurement is taken. 5 nodes max.
Reference	Pin/node number(s) of the ground reference (s). 10 nodes max.
Wait (ms)	0 to 65534 ms. Added to default wait of 3 ms typical.

Measure Modes. Test V can be done in four measure modes, DC, Peak, Peak-Peak and RMS as controlled by the measure type field.

DC	**DC voltage**
Peak	Absolute value of greatest excursion from zero in either direction
Peak–Peak	Difference between the most positive and most negative excursion
RMS	The Root Mean Square average of the measured signal. For a sine wave it equals 0.707 times the peak value

Wait Time. The Wait time field is used to specify the time between when the ATB is completely set up and when the measurement is taken. An internal relay settling time of 3 ms is applied after all relays on the ATB and driver/receiver card have closed and before the wait time applies.

For PK, PK–PK, and RMS measurements, the wait time is effectively the gate time for the detectors. For DC measurements it acts simply as a further delay after all the relays have closed. Minimum wait times are enforced depending on the measure type: they are 10 ms for PK and PK–PK, 500 ms for RMS, and 2 ms for DC. The wait time appearing on the Test Properties portion of the Step Worksheet is added to these defaults.

The effect of extending wait time depends on the measure type. For PK and PK–PK, the wait time should be at least one full cycle of the signal to be measured. Extending the time much beyond that only worsens the risk of capturing possible noise spikes and therefore distorting the reading. The 10 ms default for PK and PK–PK allows for signal measurements down to 100 Hz. Beyond that, extra wait times have to be programmed in Test Properties.

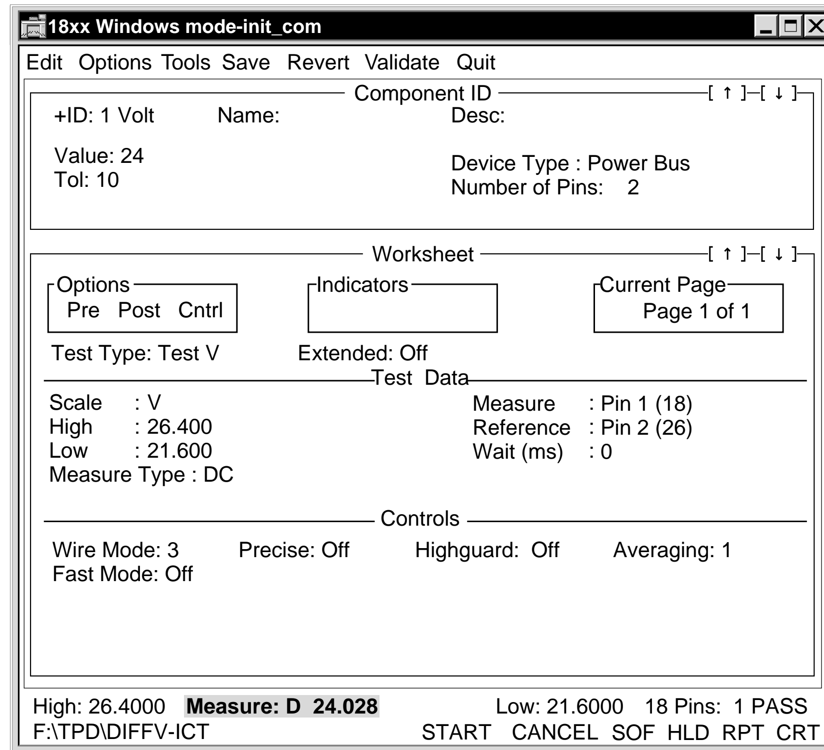
For RMS, the longer one lets the RMS converter collect input signals, the more precise and stable the result is. The minimum conversion time the RMS converter needs is 500 ms; therefore, RMS measurements have a much larger default.

Differential Measurements. As you can see from the ATB Setup for Test V Mode diagram above, the reference for the measurement is connected to the system ground via the ATB. This causes a problem when the board is powered, since the DUT power supplies are also referenced to the same system ground. (The ATB is not floating.)

For example, if on a powered board you want to measure two points that are at + 3 volts and +5 volts in respect to system ground and board-under-test ground, where the +3 V point is used as the reference point, the ATB would connect this point to system ground as well and shorts out the +3 volts. To overcome this problem, the system performs differential measurements whenever

the board under test is powered up by taking two measurements on (1) the reference point and (2) the measure point and then subtracting one from the other for the result. Differential measurements therefore take twice the time a single measurement would take.

Differential measurements require that you specify a ground reference node in the PRGMVARS Ground Reference Node field. The system indicates that it took a differential measurement by putting a D in the display line just before the result.



Be aware that differential measurements can be suppressed by listing known ground points in the program Header. When a Test V test is executed, and the reference node matches a known ground reference node out of the program Header, the system can perform a single-ended measurement instead. Also, if no reference node is specified in Test Properties, no conflict exists and a single-ended measurement is taken by default.

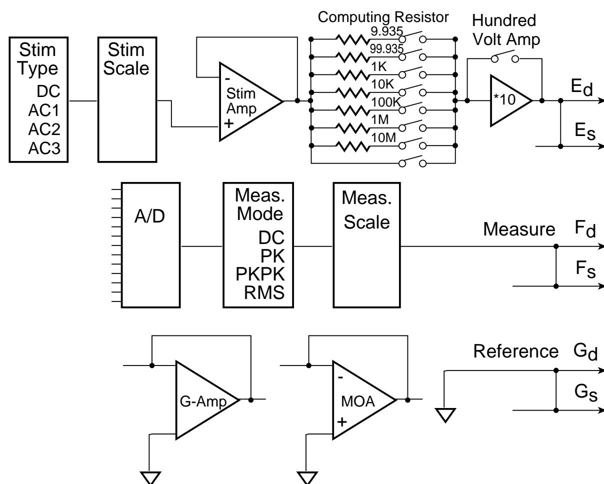
Test V and Ranges

Test V by default autoranges to higher scales until all ranges are exhausted before displaying an overrange flag.

TEST V STIM V

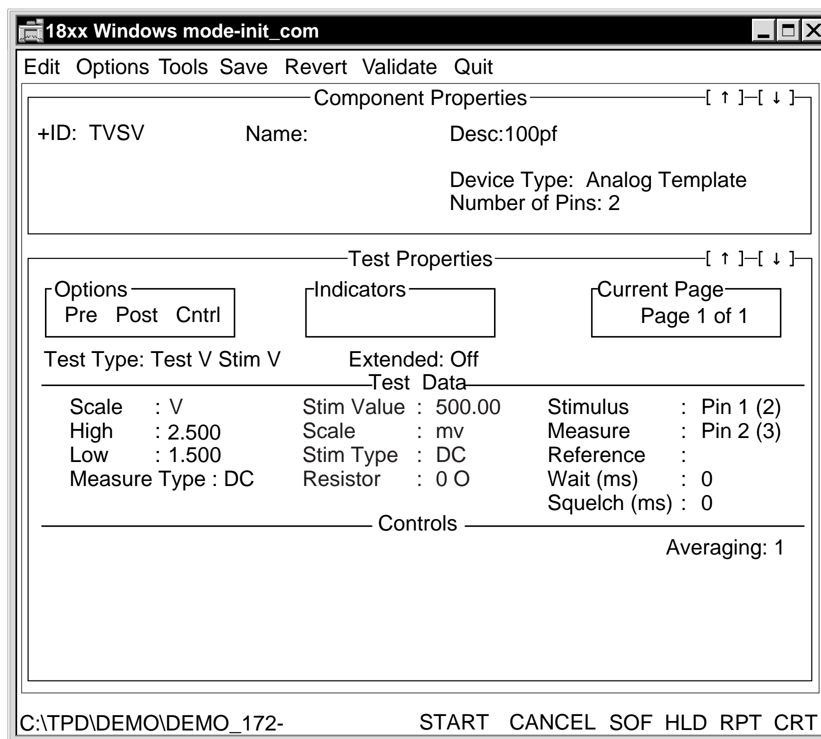
The Test V Stim V mode is an extension of the TEST V test type with an added voltage stimulus. See TEST V for a description of the measurement parameters.

The following illustration show the ATB setup for Test V Stim V.



Worksheet

The Test Properties for Test V Stim V is shown below.



Test Data for Test V Stim V /Test Properties Portion of the Step Worksheet

Test V Stim V Type:

Scale	Measurement-related modifier—uv, mv, V
High	Upper limit for a passing measurement. Range = -1000 to +1000
Low	Lower limit for a passing measurement. Range =-1000 to +1000
Measure Type	DC, Peak, RMS, or Pk-Pk (peak to peak)
Stim Value	Value of stimulus. Range =-1000 to +1000
Scale	Stimulus-related modifier—mv, V
Stim Type	DC, AC1, AC2, AC3, Ext
Stimulus	Pin/node numbers(s) to which stimulus applied. 5 nodes max.
Measure	Pin/node number(s) at which measurement is taken. 5 nodes max.
Reference	Pin/node number(s) of the ground reference (s). 10 nodes max.
Wait (ms)	0 to 65534 ms. Added to default wait of 3 ms typical.
Squelch (ms)	0 to 65534 ms. Repeatable initial condition to remove stored energy.

In addition to the Test V test type this test setup provides a voltage stimulus via the stimulus poles.

Stimulus magnitude and type. The Stim Value and Scale fields in Test Properties define the magnitude of the stimulus. The Stim Type selects:

- DC or AC sine wave stimulus

  Where AC1 equals 159 Hz, AC2 equals 1.59 Khz, and AC3 equals 15.9 Khz.
- Ext

  Where Ext stands for external oscillator. The input for this stim source can come from the connector J4 pin 8 on the front edge of the ATB and the EXT OSC pin in the fixture interface.

Stimulus impedance. The Resistor field in Test Properties controls the output impedance of the Stimulus circuit when stimulus voltages below 10 V are requested.

Stimulus greater than 10V. When a stimulus greater than 10 V is requested, the *10 amplifier (hundred volt amplifier) is switched into the stimulus path, and the resistor should be set to 0 Ohms, otherwise the resulting stimulus can be less than expected. There is no equivalent Stimulus resistor for 100 V option.

Stimulus current limit. The maximum current the stimulus amplifier can deliver is ~275 ma unless limited by a stimulus resistor. When the *10 amplifier is in effect, the minimum guaranteed output current is ~20 ma for DC and ~10 ma for AC stimulus. However, the maximum output current could be as high as 50 ma, depending on ambient temperature or the revision of the ATB.

Squelch. Squelch is a means to establish a known initial condition before the measurement takes place. It executes after all the relays involved close and before the stimulus is turned on. The system provides a minimum of 3 ms of squelch time that can be extended by the squelch field in Test Properties. Squelch can be used to discharge capacitors associated with the measurement to be taken.

TVSV Ranges

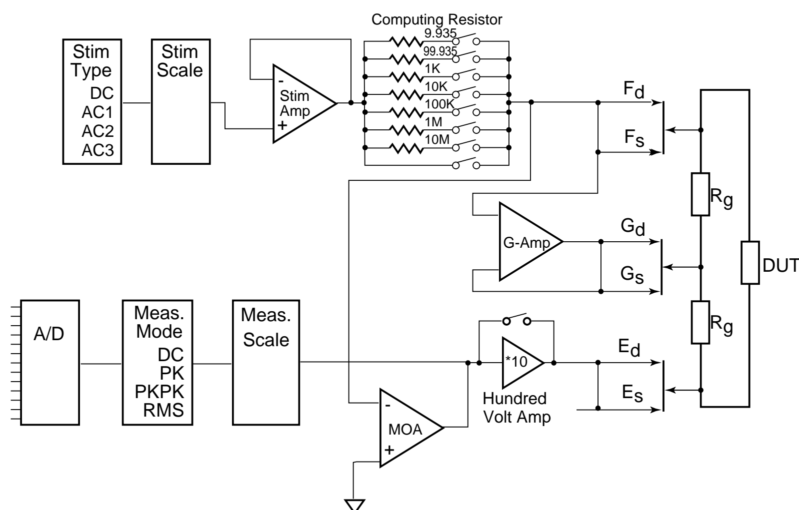
Test V Stim V by default autoranges to higher scales until all ranges are exhausted before displaying an overrange flag.

Refer to the **Z1800-Series Programmer's Guidebook**, Chapter 5, for more information about Test V, Test V Stim V Stim V tests.

Test V Stim I

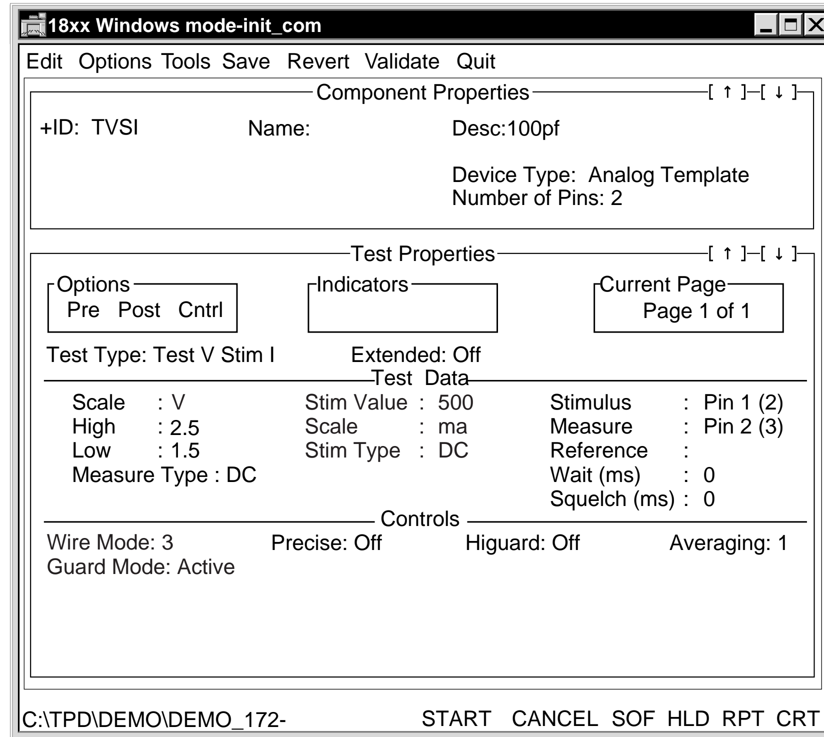
Test V Stim I measures the resulting voltage across a device under test while forcing a programmed current through it.

The following illustration shows the ATB Setup for Test V Stim I 3 Wire Precise off.



The Worksheet

The Test Properties for Test V Stim I is shown below.



Test Properties fields specific to the Test V Stim I Test Type are summarized in the table below.

Test Data for Test V Stim I /Test Properties Portion of the Step Worksheet

Test V Stim I Type:	Description
Scale	Measurement-related modifier—uv, mv, V
High	Upper limit for a passing measurement. Range = -1000 to +1000
Low	Lower limit for a passing measurement. Range =-1000 to +1000
Measure Type	DC, Peak, RMS, or Pk-Pk (peak to peak)
Stim Value	Value of stimulus. Range =-1000 to +1000
Scale	Stimulus-related modifier—na, ua, ma.
Stim Type	DC, AC1, AC2, AC3, Ext
Stimulus	Pin/node numbers(s) to which stimulus applied. 5 nodes max.
Measure	Pin/node number(s) at which measurement is taken. 5 nodes max.
Reference	Pin/node number(s) of the ground reference (s). 10 nodes max.
Wait (ms)	0 to 65534 ms. Added to default wait of 3 ms typical.
Squelch (ms)	0 to 65534 ms. Repeatable initial condition to remove stored energy.

The ATB is set up to use an inverting operation amplifier to provide Test V Stim I with the DUT in its feed back path. The stimulus amplifier and computing resistor are used to produce the programmed current.

Refer to the **Z1800-Series Programmer's Guidebook**, Chapter 5, for an explanation of the op amp theory.

Since the setup uses an inverting op amp, the resulting voltage has the opposite sign of the forced current. For example, setting up for an +1 ma current through a DUT of 1 KΩ results in a measured voltage of -1V. This holds true only for DC measurements since measurements taken with PK, PK–PK and RMS are unsigned by nature.

When programming in this mode, take care to use compatible stimulus and measurement types. For example, an AC stimulus cannot be measured with a DC measure type.

Hundred Volt Amplifier

When measurements of more than +10 V or less than -12 V are requested, the times 10 amplifier is switched into the circuit, and the maximum current it can deliver is in the area of 10–20 ma as opposed to ~275 ma without it.

Test V Stim I over Test I Stim V—Advantages/Disadvantages

Advantage. The Test V Stim I mode is preferable for capacitor testing since it suppresses noise and instability due to the placement of the capacitor under test in the feedback.

Disadvantage. The voltage across the DUT is affected by the value of the component under test. If the impedance of the DUT is higher than expected, the voltage across the DUT is also higher and might cause unguarded paths to affect the result. The worst case occurs when the DUT is entirely missing, and the MOA output swings all the way to its power supply rail, therefore putting ±13 V on the board under test. When the 100-volt amplifier is in the circuit, the maximum voltage is about 60 V.

Test V Stim I Ranges

Test V Stim I does not autorange. An overrange flag is displayed, and the test fails for measures outside of the current range.

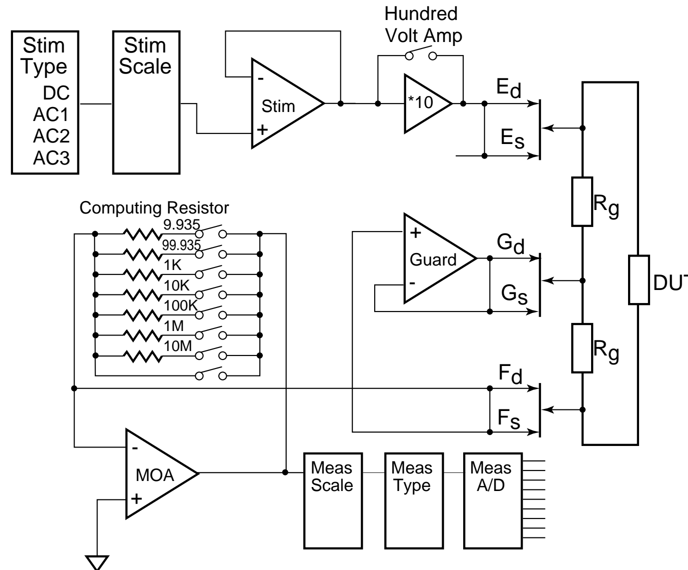
Refer to the **Z1800-Series Programmer's Guidebook**, Chapters 3 and 5, for more information about the Test Properties Controls section.

See also Test V, Test V Stim V, and Test V Stim I Stim V in this chapter.

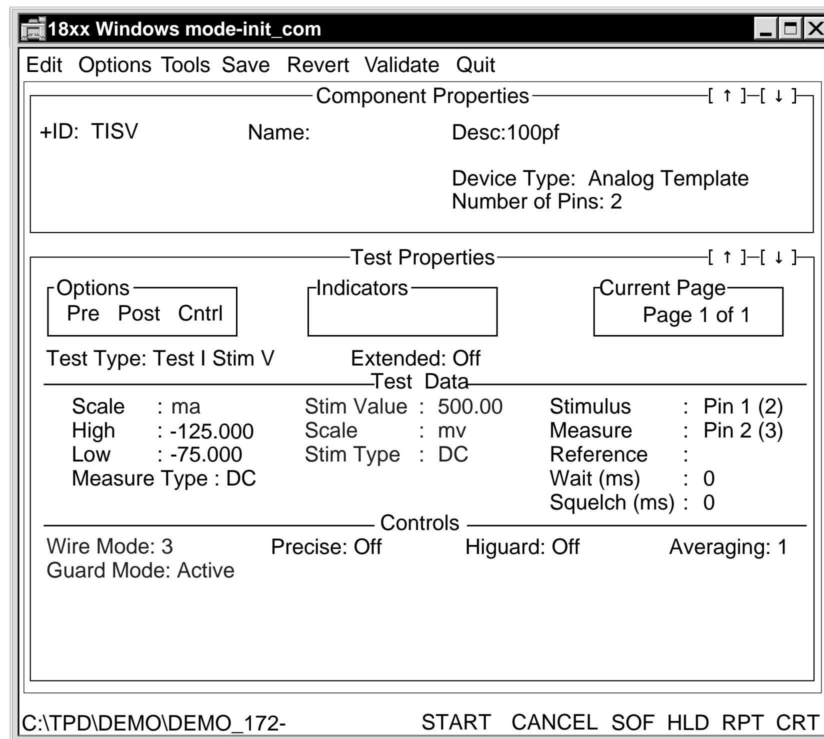
Test I Stim V

The Test I Stim V mode is the opposite of Test V Stim I. In this situation, the DUT is placed in the input leg of the MOA. While the voltage across the DUT is programmed, the current through it is measured.

The following illustration shows the Test I Stim V 3-Wire Precise Off.



The Test I Stim V Test Properties portion of the Step Worksheet is shown below.



18xx Windows mode-init_com

Edit Options Tools Save Revert Validate Quit

Component Properties

+ID: TISV Name: Desc:100pf

Device Type: Analog Template
Number of Pins: 2

Test Properties

Options: Pre Post Cntrl
Indicators
Current Page: Page 1 of 1

Test Type: Test I Stim V Extended: Off

Test Data

Scale : ma
High : -125.000
Low : -75.000
Measure Type : DC

Stim Value : 500.00
Scale : mv
Stim Type : DC

Stimulus : Pin 1 (2)
Measure : Pin 2 (3)
Reference :
Wait (ms) : 0
Squelch (ms) : 0

Controls

Wire Mode: 3 Precise: Off Higuard: Off Averaging: 1
Guard Mode: Active

C:\TPD\DEMO\DEMO_172- START CANCEL SOF HLD RPT CRT

Test Properties' fields specific to the Test I Stim V Test Type are summarized in the table below.

Test Data for Test I Stim V /Test Properties Portion of the Step Worksheet

Field	**Description**
Test I Stim V Type:	
Scale	Measurement-related modifier—na, ua, ma
High	Upper limit for a passing measurement. Range = -1000 to +1000
Low	Lower limit for a passing measurement. Range =-1000 to +1000
Measure Type	DC, Peak, RMS, or Pk-Pk (peak to peak)
Stim Value	Value of stimulus. Range =-1000 to +1000
Scale	Stimulus-related modifier—mv,V
Stim Type	DC, AC1, AC2, AC3, Ext
Stimulus	Pin/node number(s) to which stimulus applied. 5 nodes max.
Measure	Pin/node number(s) at which measurement is taken. 5 nodes max.
Reference	Pin/node number(s) of the ground reference (s). 10 nodes max.
Wait (ms)	0 to 65534 ms. Added to default wait of 3 ms typical.
Squelch (ms)	0 to 65534 ms. Repeatable initial condition to remove stored energy.
Test V Stim V Test Type:	(All of the fields above, and the following Resistor field.)
Resistor	Current-limiting resistor: 0 Ω, 10 Ω, 100 Ω, 1 KΩ, 10 KΩ, or 100 KΩ, 1 MΩ, 10 MΩ

The stimulus voltage is directly programmed and applied to one side of the DUT. The other side is held at virtual ground by the inverting measurement op amp. The Test V Stim I logic for the polarity of stimulus and measurement holds true for Test I Stim V, that is, a positive stimulus voltage will create a negative measure current.

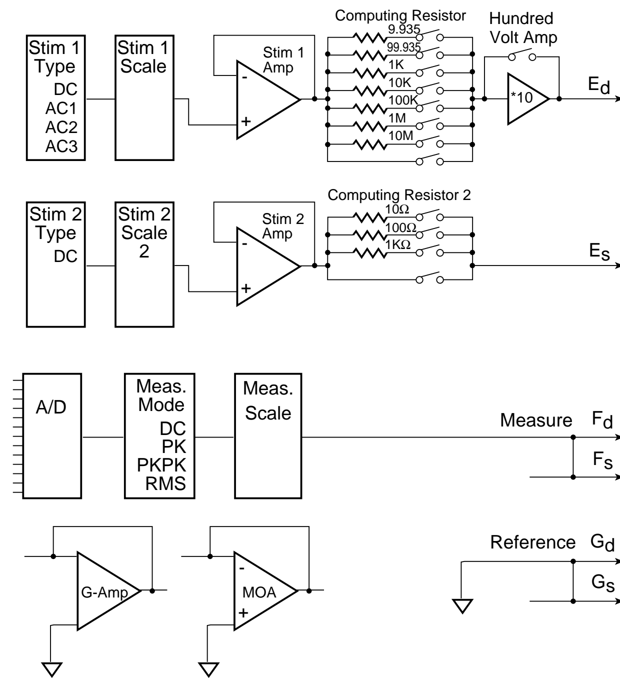
This mode doesn't have the drawback of uncertain voltage across the DUT as does the Test V Stim I method, and therefore, it is best used for resistive components. It is not a preferred mode for capacitor testing since, depending on the DUT, the Test I Stim V setup might be unstable due to inherent oscillation tendencies with capacitors in the feedback and guard path.

Refer to the **Z1800-Series Programmer's Guidebook**, Chapter 5, for more information about TV, TVSV, TVSI and TISVSV tests.

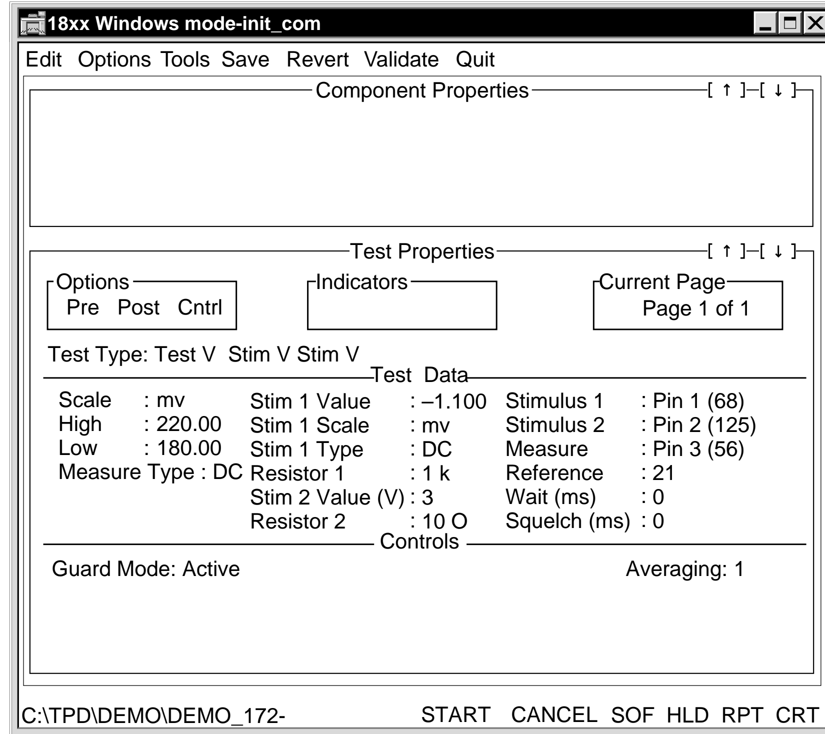
Dual Stimulus Modes

The three dual stimulus modes, TV SV SV, TI SV SV, and TV SI SV, are extensions to their related base modes providing an extra voltage stimulus. The ATB setup is modified by splitting the Stimulus pole into its drive and sense half to gain access to a fourth pole for the extra stimulus. The controls for wire mode and precise are traded off for the dual stimulus feature.

The following illustration shows the Dual Stim Mode, Test V Stim V Stim V.



The TV SV SV worksheet is shown below.



Test Properties fields specific to the Test V Stim V Stim V Test Type are summarized in the table below.

Test Data for Test V Stim V Stim V/Test Properties Portion of the Step Worksheet

Test V SV SV Type:	Description
Scale	Measurement-related modifier—uv, mv, V
High	Upper limit for a passing measurement. Range = -1000 to +1000
Low	Lower limit for a passing measurement. Range =-1000 to +1000
Measure Type	DC, Peak, RMS, or Pk-Pk (peak to peak)
Stim 1 Value	Value of stimulus 1. Range = -1000 to +1000
Stim 1 Scale	Stimulus related to modifier—mv, V
Stim 1 Type	DC, AC1, AC2, AC3
Resistor	Current limiting resistor for stimulus 2 values: 10 ohms, 100 ohms, 1K
Stim 2 Value (V)	Value of stimulus 2. Range = -6.4 V to +6.4 V
Resistor 2	Current limiting resistor for stimulus 2 values: 10 ohms, 100 ohms, 1 K
Stimulus 1	Pin/node number(s) to which stimulus 1 is applied. 5 nodes max. Range = 0–2047.
Stimulus 2	Pin/node number(s) to which stimulus 2 is applied. 5 nodes max. Range = 0–2047. Note: Stim 1 and Stim 2 nodes can't be in same group of 16 nodes.
Measure	Pin/node number(s) at which measurement is taken. 5 nodes max.
Reference	Pin/node number(s) of the ground reference (s). 10 nodes max.
Wait (ms)	0 to 65534 ms. Added to default wait of 3 ms typical.
Squelch(ms)	0 to 65534 ms. Repeatable initial condition to remove stored energy.

The second stimulus is controlled by the Stim 2 Value, Resistor 2, and Stimulus 2 pin/node fields. Stimulus 2 is a low resolution output stimulus from 0 to +6.4 V DC in 25 mv increments. You can select an output impedance of 10 Ω, 100 Ω or 1 KΩ via the Resistor 2 field. The maximum current from Stim 2 is limited to 275 ma unless limited further by Resistor 2. The stimulus is routed to the nodes specified in the Stimulus 2 pin/node field. Since the E sense/E drive poles are used, the nodes listed in Stimulus 1 and Stimulus 2 fields cannot be on the same half of the same driver/receiver board. For example if Stimulus 1 is set to node 3, Stimulus 2 cannot be between nodes 0 and 15.

The other two dual stimulus test types follow the same principles as TV SV SV, and the same restrictions apply.

Test Properties' fields specific to the Test I Stim V Stim V Test Type are summarized in the table below.

Test Data for Test I Stim V Stim V/Test Properties Portion of the Step Worksheet

Test I S V S V Type:	Description
Scale	Measurement-related modifier—na, ua, ma
High	Upper limit for a passing measurement. Range = -1000 to +1000
Low	Lower limit for a passing measurement. Range =-1000 to +1000
Measure Type	DC, Peak, RMS, or Pk-Pk (peak to peak)
Stim 1 Value	Value of stimulus 1. Range = -1000 to +1000
Stim 1 Scale	Stimulus related to modifier—mv, V
Stim 1 Type	DC, AC1, AC2, AC3
Stim 2 value (V)	Value of stimulus 2. Range = 6.4 V to +6.4 V
Resistor 2	Current limiting resistor for stimulus 2 values: 10 ohms, 100 ohms, 1 K
Stimulus 1	Pin/node number(s) to which stimulus 1 is applied. 5 nodes max. Range = 0–2047.
Stimulus 2	Pin/node number(s) to which stimulus 2 is applied. 5 nodes max. Range = 0–2047. Note: Stim 1 and Stim 2 nodes can't be in same group of 16 nodes.
Measure	Pin/node number(s) at which measurement is taken. 5 nodes max.
Reference	Pin/node number(s) of the ground reference (s). 10 nodes max.
Wait (ms)	0 to 65534 ms. Added to default wait of 3 ms typical.
Squelch (ms)	0 to 65534 ms. Repeatable initial condition to remove stored energy.

Test Properties' fields specific to the Test V Stim I Stim V Test Type are summarized in the table below.

Test Data for Test V Stim I Stim V/Test Properties Portion of the Step Worksheet

Test V S I V Type:	Description
Scale	Measurement-related modifier—uv, mv, V
High	Upper limit for a passing measurement. Range = -1000 to +1000
Low	Lower limit for a passing measurement. Range =-1000 to +1000
Measure Type	DC, Peak, RMS, or Pk-Pk (peak to peak)
Stim 1 Value	Value of stimulus 1. Range = -1000 to +1000
Stim 1 Scale	Stimulus related to modifier—na, ua, ma
Stim 1 Type	DC, AC1, AC2, AC3
Stim 2 Value (V)	Value of stimulus 2. Range = -6.4 V to + 6.4 V
Resistor 2	Current limiting resistor for stimulus 2 values: 10 ohms, 100 ohms, 1 K
Stimulus 1	Pin/node number(s) to which stimulus 1 is applied. 5 nodes max. Range = 0–2047.
Stimulus 2	Pin/node number(s) to which stimulus 2 is applied. 5 nodes max. Range = 0–2047. Note: Stim 1 and Stim 2 nodes can't be in same group of 16 nodes.
Measure	Pin/node number(s) at which measurement is taken. 5 nodes max.
Reference	Pin/node number(s) of the ground reference (s). 10 nodes max.
Wait (ms)	0 to 65534 ms. Added to default wait of 3 ms typical.
Squelch (ms)	0 to 65534 ms. Repeatable initial condition to remove stored energy.

2 BOARD POWER

You can use Board Power test steps to specify the nature of the power applied to a board for linear and digital component programs. Two types of power supply Test Properties allow you to set up parameters for applying power and measuring voltage at the device-under-test using either nonprogrammable or programmable power supplies.

The nonprogrammable power supply test steps are set up using Power Test Type listed in Test Properties. There are 7 power types available to control the application of power and measurement of power supply output. These power types control the DUT 5 volt, Adjustable A, and Adjustable B power supplies.

The programmable power supply test steps are set up using the Power Prog 5.5V, Power Prog A, Power Prog B, and Power Prog Slaved Test Properties. These programmable Test Properties control the DUT 5 volt, Programmable A (0–55 V), Programmable B (0–55 V), and optional DUT 5.5 volt power supplies.

The Power 5V Test Properties portion of the Step Worksheet does not provide programmable control over the DUT 5 volt power supply. It controls the programmable power supply controller (PN 051-002-xx) as the +5 Volts Power Type in the Power Test Properties controls the power supply controller (PN 045-047-xx).

Step Worksheet

You can edit a board power test at any time from the Step Worksheet. To access a board power Step Worksheet from the Main menu, select

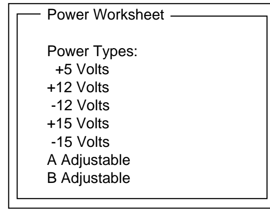
1. The board program
2. Edit
3. Brd_Power
4. The board power Step Worksheet from the Component Select window

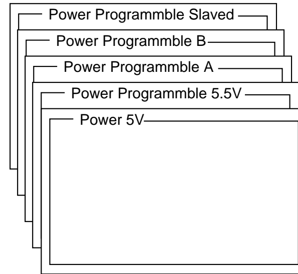
The Step Worksheet appears. At the top of the Step Worksheet is the menu bar, under that, the Component Properties portion of the Step Worksheet, and under that, the Test Properties portion.

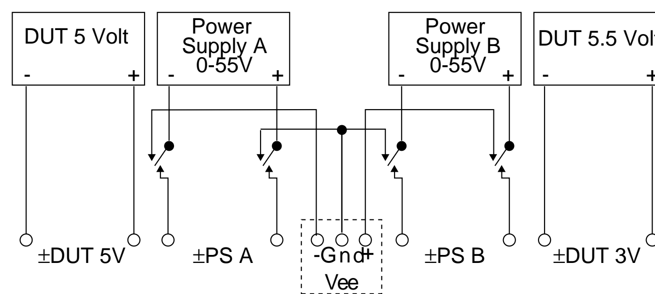
You must have the Programmable Power Supply Controller PN 51002 to use the Test Types:

- Power 5V
- Power Prog 5.5V
- Power Prog A
- Power Prog B, and
- Power Prog Slaved.

The following provides a graphic representation of the software and hardware elements involved in controlling power to 1800-series testers.



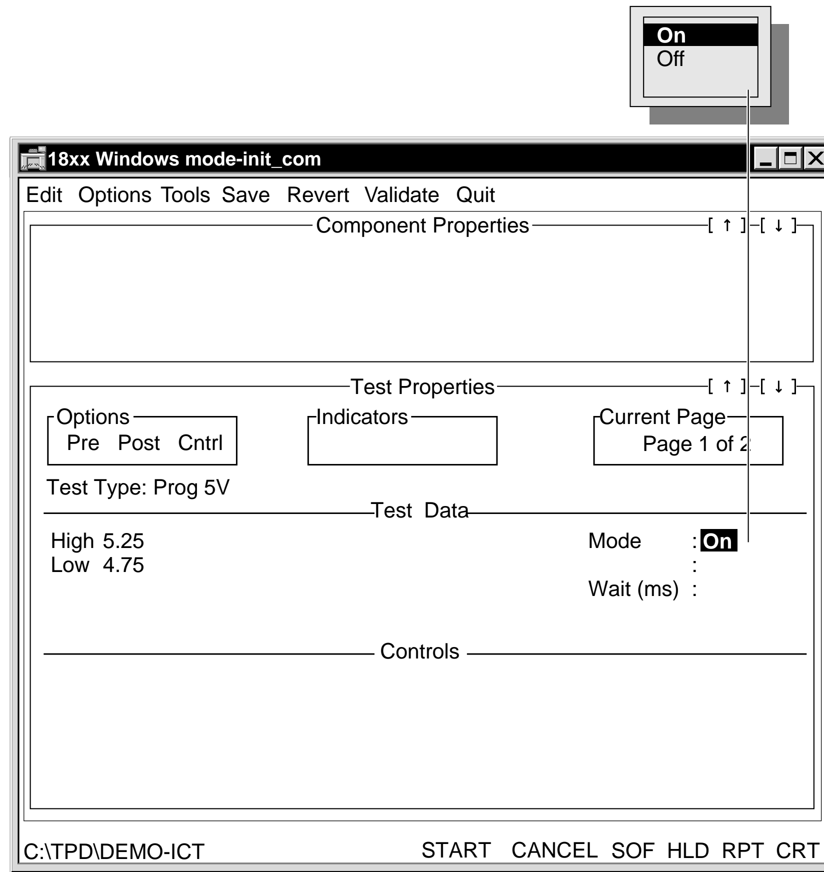




The examples on the following pages show first, a Step Worksheet for a board power test step using nonprogrammable power supplies and second, Test Properties for a board power test step using programmable power supplies.

Below is an example of a nonprogrammable power supply Step Worksheet.

Below is an example of a programmable power supply Test Properties. The Component Properties portion of the Step Worksheet is the same as for the adjustable power supply test step.



Editing Test Properties

The Test Properties portion of the Step Worksheet for both types of power supplies contains the parameters to execute the test step. The table below describes the Test Properties' fields unique to Board power.

Upper Test Properties Area

Field	Description
Test Type	Test configuration for the current Test Properties page. For board power:
No Test	No Test executed. Wait state possible, however.
Power	Shorthand power test step. Not programmable.
Power 5V	Test for DUT 5V power supply. Not programmable.
Power Prog 5.5V	Test for use with 3 V optional power supply. Programmable range 0–5.5 volts.
Power Prog A	Test for power supply A. Programmable range: 0-55 volts.
Power Prog B	Test for power supply B. Programmable range: 0–55 volts.
Power Prog Slaved	Test for slaved A and B power supplies. Programmable range: 0–55 volts.
Test V	Longhand voltage test. Also test type for second and third pages of programmable test types to measure voltage at DUT.

Test Data/ Middle Test Properties Area

PowerTestType:	For use with Power Supply Controller PN 45047
Scale	Power unit modifier—uv, mv, V.
High	Upper limit of a passing measurement.
Low	Lower limit of a passing measurement.
Power Type	Specifies power supply. Choices are: +5 Volts, +12 Volts, -12 Volts, +15 Volts, -15 Volts, A Adjustable, B Adjustable.
Measure	Pin/node number(s) at which measurement is taken. 5 nodes max.
Reference	Pin/node number(s) of ground reference point(s). 10 nodes max. If no measurement given, measurement is referenced to system ground
Wait (ms)	0 to 32000 ms. Added to default wait of 3 ms typical.
Power 5 Test Type	For use with PS controller PN 51002. Same fields as Power Prog test types, but without the Value field. Functions like Power Type +5 Volts.
Power Prog Test Types	For use with PS controller PN 51002. Power Prog A, Power Prog B, and Power Prog Slaved
Value (V)	Enter desired value, 0–55 volts for Power Prog A, Power Prog B, and Power Prog Slaved; 0–5.5 volts for 3 volt option.
High	Upper limit of a passing measurement. Always stated in actual value, not percent
Low	Lower limit of a passing measurement. Always stated in actual value, not percent.
Mode	Enables selection of connection of power supply to output pins (On/Off); disables or reenables power supply (Disable/Enable); changes voltage for programmable power supplies without changing state of connection (Reprogram).
Wait (ms)	Same as adjustable Power test type.
Test V Test Type	Contains all Power fields except Power Type.

Refer to the **Z1800-Series Programmer's Guidebook**, Chapter 3, for further details about Step Worksheet fields not discussed here.

Test Type

From the Test Types pop-up window, displayed below, you can turn on and measure a system power supply, measure just a power supply output, test with IEEE instruments, or access power steps from an external program or Lab Windows.

DigFuncProc	Power Prog 5.5V
External Program	Power Prog A
IEEE	Power Prog B
No Test	Power Prog Slaved
Power	Test V
Power 5V	

When you change Test Types, the Test Properties fields change accordingly.

No Test allows you to interact with flags and relays as you might in a normal test step, without turning on power or taking a measurement. The test type provides only a single Wait state field in Test Properties.

The Test V test type allows you to measure voltage according to the parameters stipulated in the Test Data fields.

Nonprogrammable Test Properties Editing

Nonprogrammable Power Test Properties are one-page tests that include embedded (external) measurement of the DUT nodes. The pop-up window in the Power Type field enables you to control the DUT 5 V and A and B power supplies.

The Power test type allows you to select the power supply for the test step.

+5 Volts refers to the 5-Volt DUT (device under test) logic supply. +12 Volts, +15 Volts, and A Adjustable refers to the A Adjustable power supply. -12 Volts, -15 Volts, and B Adjustable refer to the B Adjustable power supply.

You must use 12-Volt supplies together and 15-Volt supplies together. You cannot use +12 with -15, for example. For asymmetrical voltages, choose the A Adjustable and B Adjustable settings.

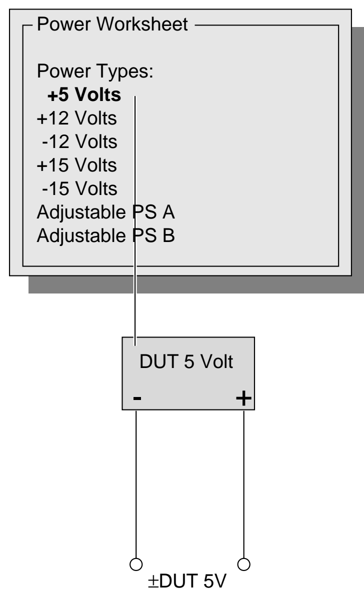
The 12- and 15-Volt fixed power supplies route to the fixture from the fixture receiver's V_{ee} pins. The A and B Adjustable supplies route to the fixture from the fixture receiver's PPSA and PPSB pins.

The Scale field allows you to change the scale or unit modifier of the measured voltage from a pop-up window. Scale represents the scale of the High and Low limits. For Power and Test V the scales are uv, mv, and V. The IEEE scales are pico, nano, micro, milli, unity, Kilo, and Mega.

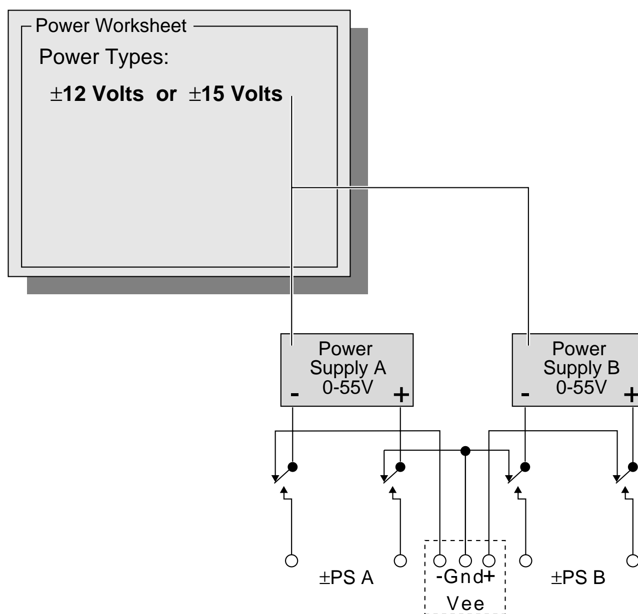
Nonprogrammable Power Type/Power Supplies

The following illustrations show how the Test Properties' Power Type relates to the power supplies.

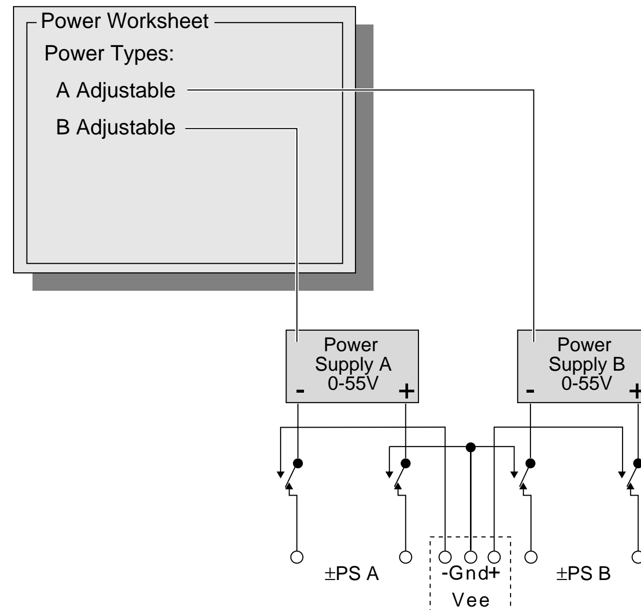
This illustrates a +5 Volt Power Type.



This illustrates ±12 Volt or ±15 Volt Power Supplies



This illustrates A Adjustable and B Adjustable Power Types.



Programmable Power Supplies—Test Properties Editing

Control of the programmable power supplies is exercised through the programmable power supply Test Properties. These two-page (Power Prog 5.5 and Power Prog A and B) or three-page (Power Prog Slaved) tests make an internal measurement of the DUT directly from the power supply in addition to controlling the application of power.

All Test Properties that control the Power Supply Controller PN 51002 have high and low fields that are used as thresholds for the internal voltage measurement. They also have a control selection with the minimum choices of On or Off (Power 5V); programmable power supplies have Enable, Disable, and Reprogram functions. In addition a Wait time is available.

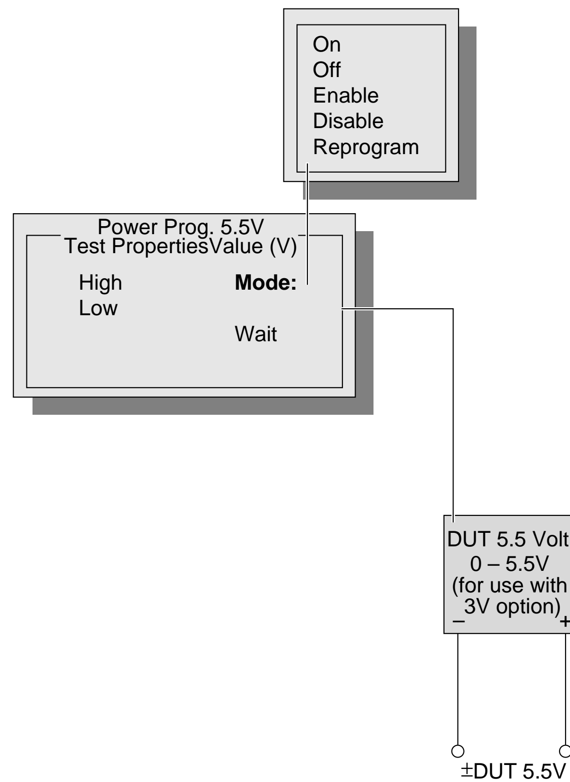
Internal Measurements—Low/High Thresholds. All power supply Test Properties that control Power Supply Controller Board PN 51002 conduct an internal measurement whenever power is turned on, enabled, or reprogrammed. The measurement path for this voltage comes directly from the power supply controller and measures the voltage directly at the output of the power supply. Depending on the placement of the sense lines and the amount of current, this voltage will vary from the voltage on the DUT. This measurement should be used to verify that the power supply is working. For all internal measurements, the low/high thresholds are derived from the requested tolerance plus 15% for an internal measurement of the supply. To precisely measure the voltage on the DUT, the Test V measurement on a subsequent page (or pages) is done to the user-specified tolerance(s).

Wait Time. The Wait time (0–32,000 ms) applies after a power supply has been turned on, enabled, or reprogrammed and before the internal measurement takes place.

Mode Control. The Mode field produces a pop-up window with the following choices:

- On—Programs, connects the power supply to the output via relays, waits, and takes an internal measurement.
- Off—Discharges and disconnects the power supply.
- Enable—Reconnects the power supply and reenables it to the same voltage specified before a Disable, waits, and takes an internal measurement.
- Disable—Disables the power supply, discharges, and disconnects the power supply.
- Reprogram—Changes the voltage for programmable power supplies without changing the state of the connection, waits, and takes an internal measurement.

The various Test Properties and their relation to the power supplies are shown in the following illustrations.



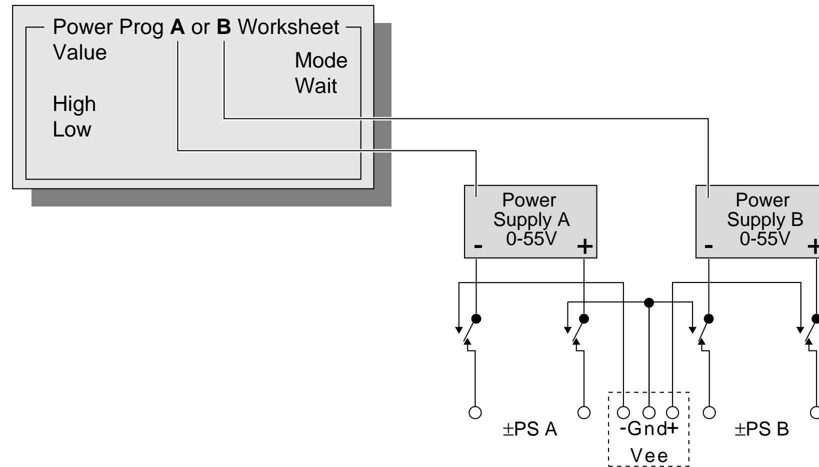
You can use the Power Prog 5.5V two-page Test Properties to control power to the DUT 5.5 V power supply that is used for the 3 Volt Option. This test is created with two test pages. Page 2 contains the Test V test to measure the voltage at the DUT.

To ensure stable test results, do not program the programmable power supply below 1 volt.

The Value field enables you to specify the voltage the power supply will be set to from 0–5.5 volts.

The High, Low, and Wait fields function as explained above.

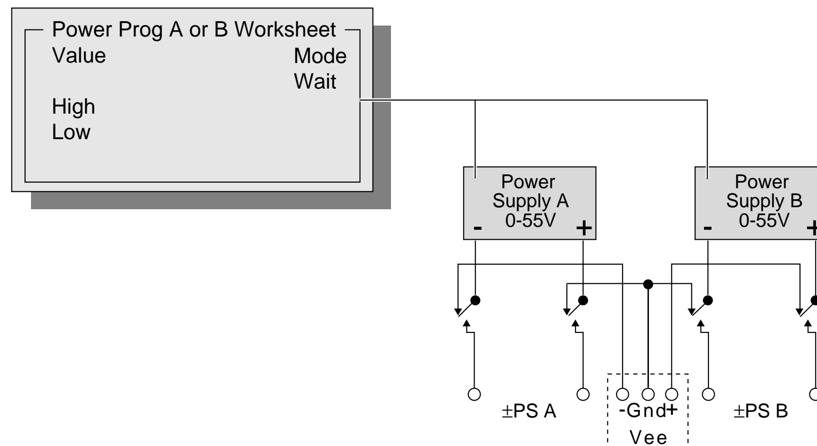
This illustrates Power Prog A or B.



The Power Prog A and Power Prog B Test Properties affect power supplies A and B respectively. The second page of the Test Properties measures the voltage at the DUT through the Vee relays.

The Value, High, Low, Mode, and Wait fields function as they do for the Power Prog 5.5V Test Properties.

This illustrates Power Prog Slaved.

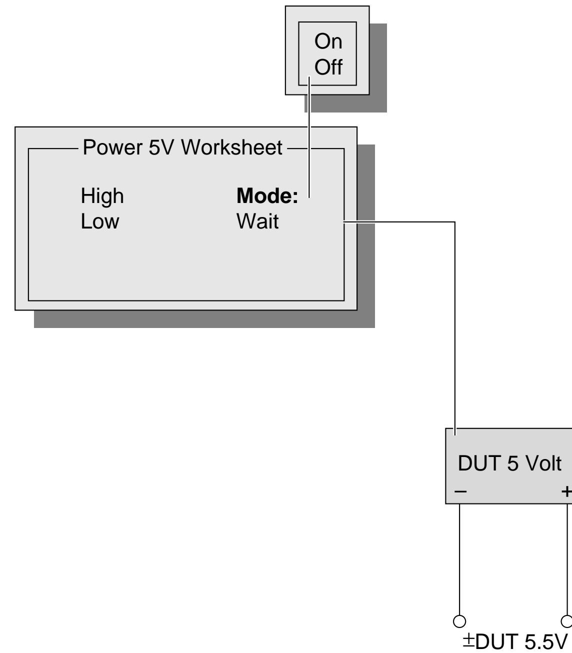


The Power Prog Slaved Test Properties enables power supplies A and B. If you use this Test Type, you cannot have a Power Prog A or Power Prog B test type in the same test.

This test type has three pages. To create the second and third pages for this test you must have the PRGSUPWS variable in the PGEN.CFG file set to Yes. To produce a Test V type of test page, use Tools/Add Page to create pages two and three.

The Value, High, Low, Mode, and Wait fields function as they do for the Power Prog 5.5V Test Properties.

This illustrates Power 5V.



The Power 5 Test Properties turns power on and off to the DUT 5 volt power supply using the programmable power supply controller PN 51002. It functions like the Power Type +5 Volts in the Power Test Properties.

The High and Low fields function as they do for Power Prog 5.5V.

Use the Power 5 Mode field pop-up window to select On or Off to connect or disconnect the power supply to the output pins via relays.

The Wait field allows you to specify a wait state from 0 to 32,000 ms. Wait happens after the power is turned on and before the internal measurement is concluded.

3 CAPACITORS

Capacitor tests can be divided into two basic modes of testing—shorthand and longhand. The shorthand modes are component-type specific and offer the best possible performance since the operating system can make certain assumptions about the component under test and about the way the test system is applied to test it.

You can use the following shorthand test modes for capacitor tests:

- Capacitor
- Extended
- Cap Phase

You can access the Capacitor and Cap Phase modes through their respective Test Types in Test Properties. To enable Extended mode, select Extended/Yes in to the right of the Test Type field in Test Properties. Each of these modes has an option for resistor/capacitor (RC) combination test.

Longhand tests, while available for capacitor testing, have certain disadvantages in that the longhand test types do not have built-in programming to automatically compensate for varying effects of board and system capacitance on the device under test.

Test Type: Capacitor Functionality

- Basic test type for capacitors from 10 pF to (end of range)
- Two modes of operation—AC or DC change up
- Fastest test type (Fast Mode On increases execution speed)
- Basic RC test capability
- Auto-ranging with Extended On
- Specifiable V_dut Pk–Pk with Extended On

Test Type: Cap Phase Functionality

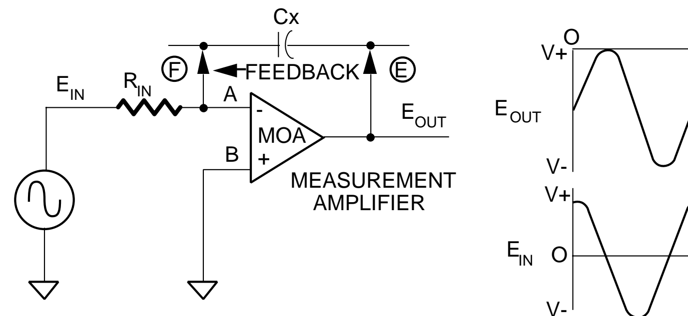
- Improved low end, single digit pF to 99.9 nF
- Improved test for RC combinations
- Improved precision and stability (speed is not as great as with the Capacitor test type)
- Test Properties Offset Cap compensates for capacitance in the fixture

The PRISM-Z (PRecision Integrated Signal Measurement) module is available as an option and can be used for Capacitor tests. Refer to the **Z1800-Series PRISM-Z User's Guide** for a complete discussion about the PRISM-Z test types available for Capacitor tests.

Capacitor Theory

The tester performs standard shorthand capacitor tests in Test V Stim I mode.

The following illustration shows the shorthand measurement configuration for capacitors (Test V Stim I).



With this ATB setup, a reference resistor is in the amplifier input leg and the DUT is in the feedback loop. The voltage stimulus source and reference resistor set the stimulus current. The ATB measures the resulting voltage across the DUT.

The tester executes capacitor tests in either AC or DC mode, depending upon the capacitor's value. (See the table on the following page.) AC tests are preferable since capacitors have low impedance due to stimulus, and are not easily influenced by unguardable parallel paths. However, for capacitors above 300 µF, the tester uses DC when DUT impedance approaches the residual series resistance. A shift in test results can sometimes be observed at the AC/DC break point. This shift is largely due to the fact that the impedance of the DUT when tested in DC mode is higher, and parallel paths affect the result more than when an AC test is done.

For capacitors below 300 µF, the tester chooses an AC stimulus and peak-to-peak measurement. AC1 is for capacitors of 1 µF and up, while AC2 is for values less than 1 µF. The AC stimulus voltage is 200 mV for 1 µF capacitors and up, and 2 V when values are less than 1000 pF. See also the extended shorthand option.

When DC tests are in effect, a constant DC current is stimulated for a specific time, and the voltage across the DUT is measured. The stimulus current and time are chosen so the resulting voltage across is about 200 mv. The E-pole (stimulus) is positive with respect to the F-pole (measurement).

Capacitor Range and Accuracy

The range column states the testable range of capacitor values. The accuracy of a test technique at a given range is opposite each row of ranges. The stimulus column displays the stimulus within the stated range.

Range	Accuracy		
	3-wire	6-wire	Stimulus*
10.00 to 99.99 pF	10 % ±3 pF	NA	2.0 V pk - pk AC2
100 to 999.9 pF	5 % ±3 pF	NA	2.0 V pk - pk AC2
1.000 to 9.999 nF	3 % ±3 pF	NA	0.2 V pk - pk AC2
10.00 to 999.9 nF	2 %	NA	0.2 V pk - pk AC2
1.000 to 300.0 μF	2 %	1 %	0.2 V pk - pk AC1
300.0 to 99,999 μF	5 %	NA	dc 1, 1 (μA) = C (μF)

*AC1 = 159.1 Hz; AC2 = 1.591 kHz

The test jacks used for viewing signals during debugging can influence small capacitor measurements. Test jacks are normally on during test execution but not during production test. To eliminate the test jack influence, turn off the test jacks in the Main Menu/Environment/Setup menu. (Waveforms are not visible with the test jacks off.)

Calculating Test Accuracy

The program generator automatically creates tests for capacitors within its range. Calculate a test's accuracy by adding the following:

- Shorthand accuracy tolerance
- System capacitance
- Guard ratio error tolerance
- Device-under-test (DUT) tolerance

Calculate the tolerance limits for a shorthand 3-wire capacitance test of 1 nF with a 20% tolerance as follows:

Shorthand tolerance (3% ±3 pF for 1 nF device)	=	±3.0%
DUT tolerance	=	±20.0%
TOTAL TEST TOLERANCE	=	±23.0%

The tester extracts system resistance (stated in Setup/Environment) from capacitors above 50 μF in AC mode.

The Setup/Environment menu contains a field for system capacitance. The default is 22 pF. The tester subtracts system capacitance from all capacitor shorthand measurements before it displays test results or compares them to programmed limits. As long as system capacitance is entered in the Setup menu, it is subtracted from the test result before the pass/fail determination is made.

The 22 pF default value is probably not correct for your particular system because of variances in fixturing and driver/receiver configurations. You should calculate your system's capacitance using the procedure outlined below in the Cap Phase Test Type section, or turn On Learn Cap Phase Offsets in PRGMVARS, General Variables.

Erroneous failures on large capacitors can occasionally occur when you are running your program from the hard disk using write-back caching. To prevent these failures, turn off write-back caching.

Step Worksheet Editing

The following illustration shows a typical capacitor Step Worksheet.

Beta
Cap Phase
CapScan
Capacitor
DigFuncProc
Diode
Discharge
External Program
IEEE
Inductor
No Test
Resistor
Test I Stim V
Test I Stim V Stim V
Test V
Test V Stim I
Test V Stim I Stim V
Test V Stim V
Test V Stim V Stim V
Transistor
Zener

APC
Analog Template
Beta-NPN
Beta-PNP
CapScan
Capacitor
DigFunProc
Diode
Discharge
Inductor
Potentiometer
Resistor
Rheostat
Rpack-DB
Rpack-DI
Rpack-DT
Rpack-SB
Rpack-SI
Rpack-ST
Transistor-NPN
Transistor-PNP
Zener

18xx Windows mode-init_com
Edit Options Tools Save Revert Validate Quit
Component Properties [↑]–[↓]
+ID: C6 Name: 1nF Desc:
Value: 1000pf Device Type: **Capacitor**
Number of Pins: 2
Tol 1: 1 Tol 2: 1
Test Properties [↑]–[↓]
Options: Pre Post Cntrl
Indicators
Current Page: Page 1 of 1
Test Type: **Capacitor** Extended: Off
Test Data
Value : 1 V_dut PK_PK (mv) Stimulus : Pin 1 (74)
Scale : nf Measure : Pin 2 (68)
High : 1.1 Guard :
Low : 0.9 Squelch (ms) 0
RC Mode Off
Controls
Wire Mode: **3** Precise: **Off** Highguard: **Off** Averaging: 1
Fast Mode : **Off** Guard Mode: **Active**
C:\TPD\DEMO-ICT START CANCEL SOF HLD RPT CRT

pf Default
nf 6 decimal
uf
mf

3
4
5
6

Active
Semi-Active
Passive

Off
On

Off
On

The tester's program execution sequence places capacitors after the global Discharge category. However, you can insert a discharge test step in a capacitor section. Select the Discharge test type in the Test Properties portion of the Step Worksheet, then identify the test step by selecting Discharge in the Test Properties Device Type field.

Component Properties

The Component Properties for capacitor test operates as it does for analog tests in general.

Field	Type	Description	Data Source*
+/•	Enable/Disable Test Step	+ Step is enabled for testing • Step is disabled for testing	Click to select.
ID:	Text. Max=8	Capacitor test step identification.	Input list ID field
Name:	Text. Max=20	Capacitor test step name	Input list CN field
Desc:	Text. Max=64	String for commenting	Input list quoted string
Value:	Text. Max=6. Pop-up	Capacitor value pf, nf, uf, mf Default, 6 decimal	Input list VAL1
Tol 1: & Tol 2:	Text	Capacitor tolerance	TOL1 and TOL2 fields
Device Type:	Pop-up**	Type of device test	C field (capacitor)
Number of Pins:	Text**. Max=128[†]	Number of device pins	NODES field

Refer to the **Z1800-Series Programmer's Guidebook**, Chapter 3, for specific details about editing Component Properties for analog tests.

Because capacitors often have asymmetric tolerances, there are two tolerance fields. Tolerance 1 (Tol 1) is the plus or high tolerance; Tolerance 2 (Tol 2) is the minus or low tolerance.

The Tol 1 and Tol 2 fields are entry fields. Highlight the fields with the cursor, and enter the appropriate one- or two-digit numbers for the respective plus and minus percent tolerance.

Test Properties

Test Properties for capacitor test operates as it does for analog tests in general except in the instances listed below in the table, Capacitor Test Properties fields.

Refer to the **Z1800-Series Programmer's Guidebook**, Chapter 3, for details about analog Test Properties fields.

Upper Test Properties Area	
Field	**Description**
Test Type:	Type of test configuration used on current Test Properties page. Recommended for capacitors:
Capacitor	For shorthand capacitor test.
Cap Phase	For testing small value capacitors and RC combinations.
Extended	Enables extended shorthand test. Default is Off.
Shorthand and Extended Shorthand Test Data Middle Test Properties Area	
Value	A numeric field specifying the nominal expected value of Scale. Range = 0 – 999.
Scale	Value field's unit modifier based on Capacitor Test Type: pf, nf, uf, mf
RC Mode	ON or OFF. When ON, activates parallel resistor/capacitor test.
V_dut Pk–Pk (mv)	A numeric field to specify voltage across the capacitor. Range = 40–800 mV. Default = 200 mV. (For extended shorthand test)
Controls/Lower Test Properties Area	
Fast Mode	ON or OFF. Default is OFF. When ON, test runs without built-in Wait and Squelch times.

Upper Test Properties Area

Test Type Field. The Capacitor Test Type is a shorthand test type that automatically configures the ATB to the Test V Stim I test mode. The appropriate stimulus frequency, limits, measurement voltage, measurement scale, and computing resistor are also selected, based on the component value and the tolerances.

The Cap Phase Test Type is a special version of the shorthand capacitor test type. Cap Phase uses a phase angle measurement to determine the capacitor value. In general Cap Phase works better than the standard capacitor measurement type for small, difficult-to-read capacitors with parallel resistance. For more information about Cap Phase testing, refer to the Cap Phase Test Type section on page 13.

Extended Field. The Extended field enables you to enable or disable extended shorthand capacitor test. This is an On/Off field with the default state being Off.

In the On state, another field is turned on in the Test Data area where you can enter the peak–peak measurement voltage in millivolts.

Test Data Area

The RC Mode field allows you to select parallel resistor/capacitor mode. Select the RC Mode field and select either On or Off. RC mode is off by default. The RC Mode field is available only in shorthand capacitor test type. It requires a shorthand resistor test on Test Properties page 1 and a shorthand capacitor test on Test Properties page 2 of the Step Worksheet.

Squelch

Refer to the **Z1800-Series Programmer's Guidebook**, Chapter 5, for detailed information about the effects of Squelch on Capacitor tests see the discussion of general analog measurement concepts.

Controls Area

The Fast Mode field, when set to On, suppresses built-in Wait and Squelch times resulting in faster test execution. Depending on the value of the component to be measured, the minimum Wait times that are built into to the system software vary from 1 to 200 milliseconds. When the Fast Mode field is set to the default Off, the test executes with the built-in Wait and Squelch times.

Extended Shorthand Test Mode

For capacitors smaller than 1000 pF, the stimulus voltage is approximately 2 V. The higher stimulus voltage prevents the use of an internal limiter circuit. If a less-than-1000 pF capacitor is missing from the board (due to a broken lead, for example), high stimulus voltage may be applied to the surrounding circuitry. In addition, the high stimulus voltage (2 V) poses a problem when testing these small capacitors in the vicinity of semiconductors that start to conduct at 0.7 V and cause a guarding problem.

To overcome both of these problems, the capacitor test has an Extended option. When the Extended option in Test Properties is On, the stimulus current is autoranged to the point that the voltage across the device under test matches the voltage requested in the V_dut Pk–Pk field in Test Properties. Then a regular capacitor measurement is performed. During autoranging, the internal limiter circuit is in effect to limit the voltage on the DUT to less than 2 V Pk–Pk. The allowable V_dut is between 40 mV and 800 mV to prevent conflict with semiconductor guarding paths.

Test Parameters

To see the actual test parameters used for a particular capacitor test, select Tools/Test Parameters. A window displays the voltages, currents, and frequency involved in the test for the currently displayed Test Properties page.

As mentioned in the foregoing discussion of capacitor testing, the ATB is set up in Test V Stim I mode for stability reasons. The stimulus (current and frequency) is chosen to yield a voltage of approximately 200 mv Pk–Pk across the DUT. However, for capacitor values below 1000pF, the stimulus is chosen in order to yield approximately 2 V Pk-Pk. A higher voltage is used to improve the signal-to-noise ratio for small capacitors. The voltage is said to be approximate since the precise value depends on the value of the capacitor under test; a smaller than expected capacitor value will result in a higher than expected voltage. This moving voltage and the fact that 2 V Pk-Pk is used for small capacitors create a guarding problem when the DUT is located in the vicinity of semiconductors such as diodes, transistors, and integrated circuits. These devices act as parallel unguardable paths as soon as the voltage reaches about 500 mv. The extended option on the Capacitor Test Properties page solves this problem by autoranging the stimulus current in order to yield the voltage across the DUT as specified in the V_dut field in Test Properties.

During the autoranging process, the maximum voltage across the DUT is limited to approximately 2 V Pk-Pk for protection of the surrounding components on the board under test. V_Dut should be programmed as high as possible but not high enough to turn on any semiconductor junctions. 300mV is a good starting value. When the autoranging process has ended, a final measurement is taken without the limiter circuit.

The autoranging effect of extended mode provides an additional benefit because a wide tolerance capacitor can be tested without losing precision at either end of the thresholds.

Drawbacks

Extended mode test takes slightly longer than regular shorthand because of the autoranging involved.

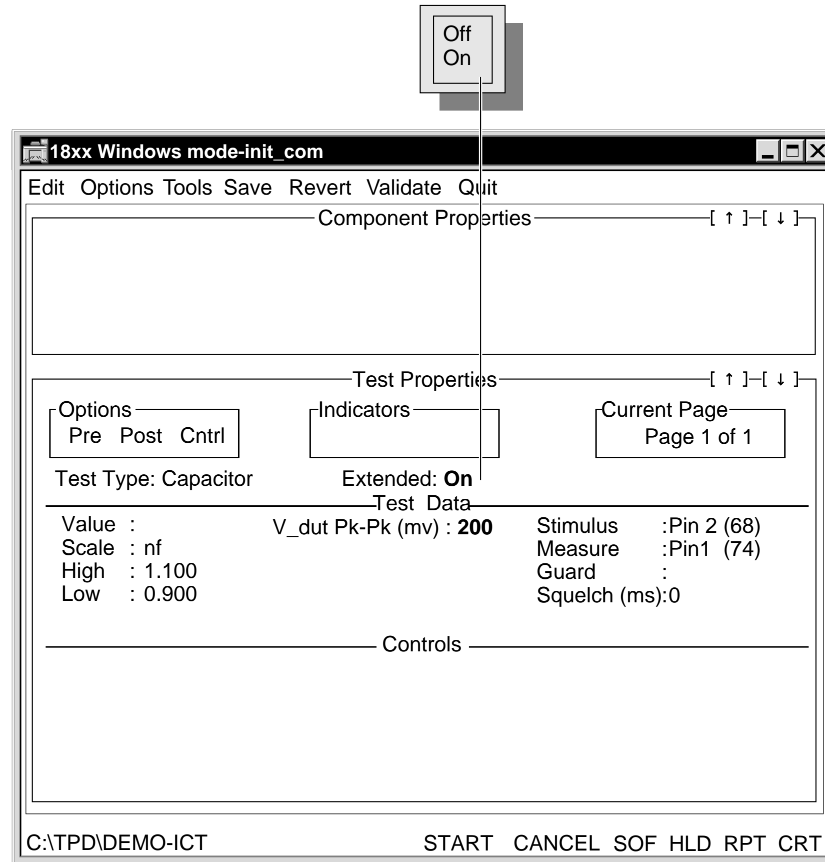
Extended mode is applicable only for capacitors measured with the AC technique used for capacitors from 10pF to 300uF.

There is no extended option available for the Cap Phase test type.

Worksheet Editing

The extended shorthand mode uses all of the test page fields as described above in the shorthand test editing section plus two others: the Extended field and the V_dut Pk–PK field.

The Extended field in the upper area of Test Properties allows you to enable or disable the extended mode for capacitor test. It is an On/Off field, with the default state being Off.



In the On state, another field in the Test Data area of Test Properties is enabled allowing you to specify the measurement voltage, in millivolts.

The extended shorthand capacitor mode field V_dut Pk–Pk is enabled when the Extended mode field is turned on. It enables you to specify a measurement peak–peak voltage other than the default voltage (usually 200 mv Pk–Pk as the lower limit) used by the system software. The system software still specifies the measurement (Pk–Pk) and stimulus types (AC), and the computing resistor.

Cap Phase Test Type

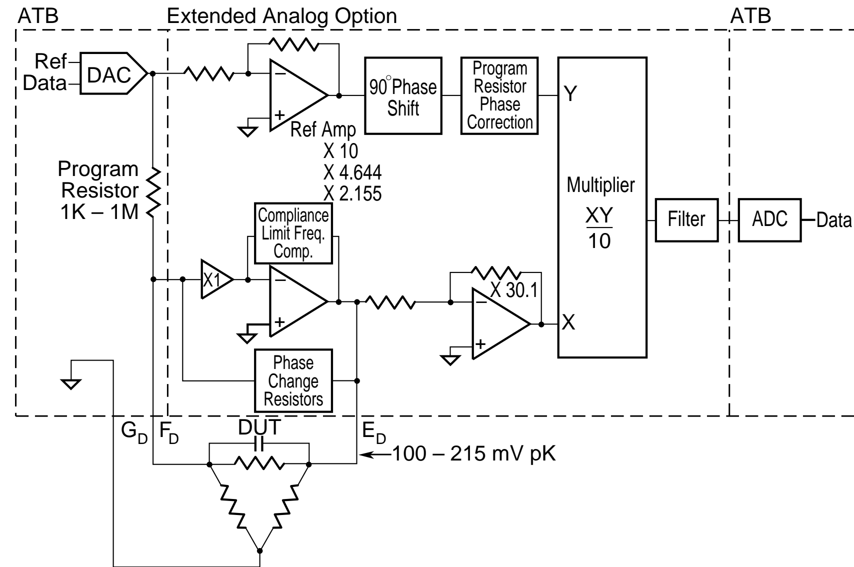
The Extended Analog Assembly (EAA) (formerly referred to as the Extended Analog Option—EAO) allows for greatly improved precision and stability in testing of small capacitor and RC combinations. Enhancements include

- Measurement as low as 2pF
- Improved reading stability
- Measurement with a parallel resistor range extended approximately 100 times

Although the RC-Phase board (Extended Analog Assembly) by means of the Cap Phase test type enables you to choose a more precise measurement technique for small capacitors and RC

combinations, the increased accuracy does affect speed. The overall range for small capacitors is single digit pF to 99.9 nF. On RC combinations, the range is specified in bulk impedance at a frequency of AC3 (15.59 kHz); the range is from 333 kΩ to 21.5 Ω. The technique permits testing to tight tolerances of a few percent.

For following illustrates an ATB Cap Phase Mode Block Diagram.



EAA Specifications

Stimulus

Open circuit voltage	Approx. 700mV
Nominal DUT voltage	<215mVp
Frequency	15.915 kHz (AC3)

Guard

Poles	3-wire only
Reference	GND
Max. guard current	<30mA
Min. guard impedance	>20Ω at 15.915kHz
Max. guard capacitance	5nF

Phase angle must be > 45 degrees at 1MHz

Error Messages

Tests will not run if an error condition is detected. The DUT TC/Phase Angle too low error can be overridden by adjusting the low test limits to a TC > 100ns. However, there is a danger of failing good components.

DUT TC Phase Angle Too Low	(<100ns)
DUT C Plus Csys Too Low	(<33pF)
DUT Z Too Low	(<90Ω)
DUT Z Too High	(>300kΩ)

Capacitor

Tolerance is for the total measured capacitance that includes both the system capacitance and the DUT capacitance.

Range 7pF to 99.9nF

(System capacitance and DUT capacitance combined must be >33pF.)

Accuracy
18XX 5% ±2pF
1884 or 18XX with DR1 or DR2P 7% ±3pF
Stability 0.5% ±0.1pF
System capacitance Approx. 40pF subtracted

Resistor/Capacitor

Tolerance is for the total measured capacitance that includes both the system capacitance and the DUT capacitance.

Range
Capacitance 7pF to 99.9nF

(System capacitance and DUT capacitance combined must be > 33pF.)

Impedance 90Ω to 300kΩ
Resistance ≥100Ω

Capacitance Accuracy

Phase	C_{low}	TC	Accuracy	
			18XX	**1884 or 18XX with DR1 or DR2P**
>45°	>7pF	>10µs	6% ±3pF	7% ±3pF
>5.71°	>10pF	>1.0µs	8% ±5pF	No Change
>2.86°	>15pF	>500ns	12% ±7pF	No Change
>1.15°	>25pF	>200ns	18% ±10pF	No Change
>0.573°	>35pF	>100ns	25% ±12pF	No Change

Phase = arc tan (Rdut/Xc)
Where: Xc = 1/100,000 Cdut
C_{low} = lowest capacitance that can be measured in the range combined with SysCap.
TC = (Csys + Clowtol) * Rdut
Where: Csys = Measured System capacitance
Clowtol = Lower limit of capacitor measure tolerance
Rdut = Measured DUT resistance
Stability 0.5% ±0.1pF
System Capacitance Approx. 40pF subtracted
Resistor Accuracy Standard ATB accuracy

Resistor/Capacitor Tolerance Calculation

1. Calculate the Time Constant (TC).

   TC = Rdut value* Cdut value
2. Determine the appropriate range.

   Example: If TC ≥ 200ns, use range >200ns.
3. Determine the typical Csys.

   Csys will typically be in the range of 33pF to 55pF. You can measure system capacitance by doing a Learn Cap or by measuring typical system capacitance.
4. Calculate the low tolerance of capacitor test.

   Example: If TC ≥ 200ns

   Clowtol = Cdut – ((Cdut*Ctol) – ((Cdut + Csys)* 18%)) –10pF

   where Ctol is the tolerance of Cdut
5. Calculate the TC for Clowtol.

   TClow = (Csys + Clowtol)*Rdut
6. If TClow is > 100ns, proceed; otherwise the test may not be possible.
7. Calculate the high tolerance of capacitor test.

   Example: If TC ≥ 200ns

   Chightol = Cdut + ((Cdut*Ctol) + ((Cdut + Csys)*18%)) +10pF

Typical Measurement Accuracy

Assumes: Csys = 40pF, No Cdut tolerance included

DUT R/C	Phase	TC	Capacitor Tolerance
10pF	NA	NA	5.5–14.5pF
1.0M/10pF	>45°	>10µs	4.0–16pF
100k/10pF	>5.71°	>1µs	1.0–19pF
50k/10pF	>2.86°	>500ns	Clow = 15pF
20k/10pF	>1.15°	>200ns	Clow = 25pF
10k/10pF	>0.573°	>100ns	Clow = 35pF
100pF	NA	NA	91.0–109pF
100k/100pF	>45°	>10µs	88–111pF
10k/100pF	>5.71°	>1µs	83–116pF
5k/100pF	>2.86°	>500ns	76–124pF
2k/100pF	>1.15°	>200ns	65–135pF
1.1k/100pF	>0.573°	>100nµs	53–147pF
1nF	NA	NA	0.946–1.054nF
10k/1nF	>45°	>10µs	0.935–1.065nF
1k/1nF	>5.71°	>0µs	0.912–1.088nF
500/1nF	>2.86°	>500ns	0.868–1.132nF
200/1nF	>1.15°	>200ns	0.803–1.197nF
140/1nF	>0.573°	>100nµs	0.728–1.272nF

RC (Resistor/Capacitor) Testing

Capacitors connected in parallel with resistors frequently appear on printed circuit boards. The tester provides a method of testing these resistor/capacitor (RC) networks in two parts using the shorthand Capacitor Worksheet as the basis for the test.

During autogeneration of an entire test program, Pgen looks for RC combinations. If a resistor is found in parallel to a capacitor, the following automatically happens:

- The capacitor test is moved to a second page.
- The resistor test is copied from the resistor section into the vacated page number 1 in the capacitor section.
- The original resistor test is disabled in the resistor section but is left there for documentation purposes.

The first page of an RC test measures the resistive component of the combination and records the result internally. When debugging RC test combinations, you must measure the resistive component as precisely as possible by using wait times, averaging, and guarding to the full extent since the result of the measurement directly affects the precision of the following capacitor test.

There is an impedance ratio beyond which the resistor is ignored, and only a capacitor, not an RC, test is generated.

The second page contains a capacitor test (Capacitor or Cap Phase test type) with the RC Mode set to On. When this test is run, the result is mathematically modified with the previously measured resistive component to extract the capacitive component.

The extraction is most successful when the bulk impedance is dominated by the capacitor, that is, when the phase angle between the current going through the resistor and the capacitor is large. The extraction becomes increasingly difficult as the phase angle decreases. Phase angle is a function of the component values involved and the stimulus frequencies.

Capacitor measurements made using the Capacitor test type are generally done with AC1 and AC2. Capacitor measurements made using the Cap Phase test type are exclusively done with AC3, which improves RC test capability

Theory

The EAA uses a phase measurement technique to extend the range of capacitors and parallel RC combinations beyond what ATB can provide with its impedance measurement approach. The EAA operates at 15.915 kHz exclusively.

When phase detection is used, the ATB stimulus DAC is programmed to provide one of three voltages: 1.0 V, 2.155 V, or 4.644 V. The stimulus follows two paths through the circuit: the reference path and the measurement path. See Figure 7.14.

The reference path provides a 10 Vp signal to the Y input of the multiplier, which is 90 degrees out of phase with the stimulus. The stimulus feeds an amplifier with three gain settings. One gain setting is selected to produce the 10 volt peak signal. This signal is phase-shifted 90 degrees, then phase-compensated to ensure 90 degree phase shift with each of the four range programming resistors.

The measurement path connects the stimulus to the F_D pole through one of the range programming resistors. The F_D pole also connects to the DUT and to the summing junction of the EAA measurement op amp. The EAA measurement op amp output connects to the other side of the DUT through the E_D pole. The DUT is placed in the amplifier feedback loop in the same fashion as the ATB's Test V Stim I configuration. The voltage across the DUT will vary from 100 mVp to 215 mVp, depending on the nominal DUT value. A 0.7 Vp compliance limit protects the DUT and surrounding circuitry from either missing or wrong value components.

The wide bandwidth EAA measurement op amp introduces negligible phase error, and is a key element in allowing effective phase measurement. Its output drives an X30.1 amplifier, which connects to the X input of the multiplier. The output of the multiplier is filtered to remove any AC components. The resulting DC voltage is proportional to the current flowing through the capacitor being measured. The ATB measures this DC voltage.

Cap Phase for Capacitor and RC Tests

Testing a component using Cap Phase is similar to testing using the Capacitor test type with the exception that you can specify capacitance offsets for each test step in the Test Properties portion of the Step Worksheet.

Test Properties for Cap Phase is very similar to Test Properties for the conventional capacitor test except for the addition of the Offset Cap (pf), Use Sys Cap, and Circuit Offset (pf) fields and the removal of control fields that are not applicable to Cap Phase test. The Offset Cap (pf) and Use Sys Cap fields allow you to control the subtraction of stray capacitance in the system and fixture. When Use Sys Cap is on (Yes), system capacitance as defined in the Setup/Environment menu is subtracted from the test result to compensate for back plane capacitance in the test system. The Offset Cap (pf) field enables you to specify a value to hold the parasitic capacitance of the fixture wiring and trace capacitance of the board under test.

The Circuit Offset (pf) field allows you to enter the stray capacitance contributed to the measurement of the DUT from the surrounding circuitry of the DUT. The Circuit Offset field also allows you to use the Value field for the actual component value and the Offset Cap field for the Fixture and System contributions to the measurement.

An independent feature associated with the Offset Cap (pf) field is Learn Cap Phase Offsets that can be turned on in the Header PRGMVAR menus.When enabled, this feature will learn the system capacitance for Cap Phase tests automatically at runtime and store the measurements in the Offset Cap (pf) field.

Refer to the **Z1800-Series Programmer's Guidebook**, Chapter 3, for additional information about Learn Cap Phase Offsets.

Creating a Test using Cap Phase Test Type

To create a test for small capacitors using the Cap Phase Test Type:

1 From a Capacitor Test Properties page, select Cap Phase from the Test Type menu.

A Test Properties page similar to the following appears.

18xx Windows mode-init_com
Edit Options Tools Save Revert Validate Quit
Component Properties
+ID: 100pf Name: 100pf Desc:100pf
Value: 100.00pf Tol 2: 5 Device Type: Capacitor
Tol 1: 5 Number of Pins: 2
Test Properties
SelectedOptions
Current Page
Page 1 of 1
Test Type: Cap Phase
Test Data
Value : 100.00 Offset Cap : 0 Stimulus : Pin 1 (0)
Scale : pF Use Sys Cap : No Measure : Pin2 (7)
High : 105.00 Circuit Offset (pf) : 0.0000 Guard :
Low : 95.000 Squelch : 0
RC Mode : Off
Controls
Averaging: 1
High: 105.0000 Measure: 98.390 Low: 95.0000 pF Node: 7 Pin: 2 PASS
C:/TPD/KMAR1 - ICT START CANCEL SOF HLD RPT CRT

2 Modify in the Value, Scale, and Tolerance fields as necessary.

Be aware that you should not specify wide tolerance ranges when using Cap Phase. Wide tolerances make it necessary for the analog circuits to be setup to accept a wide range of measurement values that will decrease accuracy and stability.

3 If you are creating an RC test, click the RC Mode field, and select Yes from the pop-up window.

4 Select the Offset Cap (pf) field to specify the offset capacitance.

5 If you want to add the system capacitance to the value subtracted from the test result, click Use Sys Cap, and select *Yes* from the pop-up window.

6 In necessary, enter the capacitance offset in the Circuit Offset (pf) field.

Range is from -1000 to +1000. Default is 0.000.

7 Select Save to save your edits.

Error Messages

An error message tells you why a test cannot be executed. Cap Phase error messages are:

- Phase mode: Impedance too high to conduct measurement.
- Phase mode: Impedance too low to conduct measurement.
- Phase mode internal error: Unable to measure.
- Phase mode: Measured values too far off expected value.

There are no remedies for these sorts of errors.

Determining System and Offset Capacitance

System capacitance is a function of the number and types of driver/receiver boards. Therefore, it is likely to be different for different test systems. Every time you make modifications to your test system, you should relearn the system capacitance and enter that value in the Setup/Environment menu. The system capacitance default value of 22 is merely a default and is probably not correct for your particular system. The procedure for calculating system capacitance is outlined below.

The offset capacitance Test Properties is a function of the fixture wiring, the layout of the traces on the board under test, and the relative node numbers involved in the particular test. Should any of these items change, you should relearn the offset capacitance.

For Cap Phase test, the two capacitative offsets are kept separate to facilitate moving a program from one test system to another without the necessity of debugging small capacitor tests again while still being able to compensate fully the parasitic wiring capacitance.

Use the following procedures to find the appropriate value for system capacitance to specify in the Setup/Environment menu and the offset capacitance to specify in the Cap Phase Test Properties.

Environmental System Capacitance

To determine environmental system capacitance

1. Using the Cap Phase Test Properties, set Offset Cap to 0, set Circuit Offset to 0, and Use Sys Cap to No.
2. Set the High value to 100 pF and the Low value to 80 pF.
3. Set the RC Mode to Off.
4. Set the Stimulus field in Test Properties to Nodes, making sure not to specify any node numbers.

   To do this, click the Stimulus field. When the Stimulus Nodes window appears, click in the parentheses to the left of Node Numbers and leave the parentheses to the right empty.
5. Set the Measure field in Test Properties to Nodes, making sure not to specify any node numbers.
6. Set the Guard field in Test Properties to Nodes, making sure not to specify any node numbers.
7. Press Start.

   The result shown is the system capacitance.
8. Enter the value in the Sys Cap field in the Setup/Environment menu.

   Refer to the **Z1800-Series Programmer's Guidebook**, Chapter 2, for more information about the Setup/Environment menu.

Offset Capacitance

After you have entered the value for system capacitance in the Setup/Environment menu, return to Test Properties for the component under test to determine the Offset Cap.

1. Click the Use Sys Cap field and select Yes.
2. Set Offset Cap to 0.0 and Circuit Offset to 0.0.
3. Set the High value to 100 pf and the Low value to 80 pf.
4. Make sure that the Stimulus and Measure fields show the appropriate test nodes or pins for the actual test to be offset.
5. If a bare board is available, place it on the fixture and apply vacuum.

   If a bare board is not available, remove the board under test from the fixture.
6. Ensure that the fixture is engaged on the interface.
7. Press Start.

   The test result is the parasitic capacitance from the system to the DUT.
8. Enter the resulting value in the Offset Cap field.

Extended Analog Assembly Specs

Tolerance is for the total measured capacitance that includes both system capacitance and DUT capacitance.

Capacitor	
Range	2 pF to 99.9 nF (System capacitance and DUT capacitance combined must be >33 pF.)
Accuracy	5.0% ±2 pF
Stability	0.5% ±0.1 pF
System Capacitance	Approximately 40 pF subtracted

Tolerance is for the total measured capacitance that includes both system capacitance and DUT capacitance.

Capacitor/Resistor		
Range	Capacitance	3 pF to 99.9 nF
	Impedance	90 ohms to 250 kohms (40 pF Sys Cap p/o Z)
	Resistance	100 ohms

.

Accuracy—Capacitor		
	Phase (Degrees)	
	>45	6% ± 3 pF
	>5.71	7% ± 5 pF
	>2.861	12% ± 7 pF
	>1.15	18% ± -10 pF
	>0.573	25% ± 12pF

Phase = arc tan (Rdut/Xc)
Xc = 1/100,000 Cdut

Stability	1% ± 0.5 pF
System Capacitance	Approximately 40 pF subtracted
Accuracy—Resistor	Standard ATB accuracy
Stimulus	
Open Circuit Voltage	Approximately 700 mVp
Nominal DUT Voltage	<215 mVp
Frequency	15.915 kHz (AC3)
Guard	
Poles	3-wire only
Reference	GND

Resistor/Capacitor Testing

Capacitors connected in parallel with resistors frequently appear on printed circuit boards. The tester provides a method of testing these resistor/capacitor (RC) networks in two parts using the shorthand capacitor Step Worksheet as the basis for the test.

During autogeneration of an entire test program, Pgen looks for RC combinations. If a resistor is found in parallel to a capacitor, the following is automatically done for you:

- The capacitor test is moved to a second page.
- The resistor test is copied from the resistor section into the vacated page number 1 in the capacitor section.
- The original resistor test is disabled in the resistor section but is left there for documentation purposes.

The first page of an RC test measures the resistive component of the combination and records the result internally. When debugging RC test combinations, you must measure the resistive component as precisely as possible by using wait times, averaging, and guarding to their full extent since the result of the measurement directly affects the precision of the following capacitor test.

There is an impedance ratio beyond which the resistor is ignored, and only a capacitor, not an RC, test is generated.

The second page contains a capacitor test (Capacitor or Cap Phase test type) with the RC Mode field set to On. When this test is run, the result is mathematically modified with the previously measured resistive component to extract the capacitive component.

The extraction is most successful when the bulk impedance is dominated by the capacitor, that is when the phase angle between the current going through the resistor and the capacitor is large. The extraction becomes increasingly difficult as the phase angle decreases. Phase angle is a function of the component values involved and the stimulus frequencies.

Capacitor measurements done using the Capacitor test type are generally done with AC1 and AC2. Capacitor measurements done using the Cap Phase test type are exclusively done with AC3, which improves RC test capability.

Please refer to the following lists.

Capacitor Value (C)	Resistor Value (R)	Capacitive Reactance (Xc)	RC Parallel Impedance (Z)	Phase Angle Degrees
100 pF	None	100 K	100.00 K	90.000
100 pF	10 M	100 K	99.995 K	89.427
100 pF	5 M	100 K	99.980 K	88.854
100 pF	2 M	100 K	99.875 K	87.138
100 pF	1 M	100 K	99.504 K	84.289
100 pF	500 K	100 K	98.058 K	78.690
100 pF	200 K	100 K	89.443 K	63.435
100 pF	100 K	100 K	70.711 K	45.000
100 pF	50 K	100 K	44.721 K	26.565
100 pF	20 K	100 K	19.612 K	11.310
100 pF	10 K	100 K	9.9504 K	5.7106
100 pF	5 K	100 K	4.9938 K	2.8624
100 pF	2 K	100 K	1.9996 K	1.1458
100 pF	1 K	100 K	999.95 Ω	0.5729
100 pF	500 Ω	100 K	499.9938 Ω	0.2865
100 pF	200 Ω	100 K	199.9996 Ω	0.1146
100 pF	100 Ω	100 K	99.99995 Ω	0.0573

DUT R/C	EAA Specification
10 pF	5.5-14.5 pF
10 pF/1.0 M	4.0-16 pF
10 pF/100 K	1.5-18 pF
10pF/10 K	0.0-24.0 pF
100 pF	91.0-109.0 pF
100 pF/100 K	88.6-111 pF
100 pF/10 K	85.2-115 pF
100 pF/1 K	53.0-147.0 pF
1 nF	0.946-1.054 nF
1 nF/10 K	0.935-1.065 nF
1 nF/1 K	0.922-1.078 nF
1 nF/100Ω	0.728-1.272 nF
10 nF	9.50-10.50 nF
10 nF/1.00 K	9.39-10.61 nF
10 nF/100Ω	9.27-10.71 nF
90 nF	85.0-95.0 nF
100 nF/200Ω	84.6-95.4 nF

DUT R/C	EAA Stability
10 pF	+-0.2 pF
100 pF	+-0.6 pF
1 nF	+-5.1 pF
100 pF/100 K	+-1.5 pF
100 pF/10 K	+-1.5 pF
100 pF/1 K	+-1.5 pF

Specifications

ATB specifications for RC testing are as follows:

Resistor range	>=10	
Capacitor range	>=1 nF <=299 µF	
Phase angle	>=45 degrees at 159 Hz or 15.9 kHz	
	(an RC time constant >=10 µS)	
Accuracy	<=99.9 nF	10% ±100 pF
	>=100 nF	20%

The Cap Phase test type makes it possible to perform RC tests on low value capacitors in parallel with resistors greater than 100 Ω. The specifications are as follows:

Capacitance	3 pF to 99.9 nF
Impedance	90 ohms to 250 kohms
Resistance	100 ohms

.

Accuracy		
	$>45^{\circ}$	6% ± 3 pF
	$>5.71^{\circ}$	7% ± 5 pF
	$>2.86^{\circ}$	12% ± 7 pF
	$>0.573^{\circ}$	25% ± 12pF

Residual Charges in Large Capacitors

Residual charges after a test has completed can pose a potential problem for further tests later on in the program. To prevent possible damage to the hardware, you can add a discharge test page to capacitor test to ensure that the capacitor will be discharged at the end of its test. For very large capacitors (above 1000 µf), which don't have a discharge path on the board under test, a fixture-mounted resistor controlled by a user relay should be added. The relay connects the resistor across the capacitor during testing of other components and is programmed to open during the test of the capacitor itself. Use the NC (normally closed) pins of a user relay and control it with Pre-/Post-Test options around the capacitor test.

Longhand Capacitor Tests

Although not recommended, capacitor test can be done with the longhand test type Test V Stim I. Test I Stim V mode is not suitable because of the inherent stability problems associated with capacitors placed in the input leg of the measurement amplifier.

Programming

To program a capacitor test in TVSI mode, you need to calculate the expected impedance of the component using the following formula.

$$Xc = \frac{1}{2 \cdot Pi \cdot F \cdot C}$$

where Pi = 3.14159
F = stimulus frequency in Hz
C = capacitance in Farad
Xc = impedance in Ohms
Or abbreviated as

$$Xc = \frac{1}{Omega \cdot C}$$

where Omega AC1 = 1000
Omega AC2 = 10000
Omega AC3 = 100000
C = capacitance in Farads
Xc = impedance in Ohms

Then calculate the stimulus current to yield a certain test voltage according to Ohms law.

$$Istim = \frac{\text{V_dut expected}}{\text{Xc expected}}$$

where Istim = peak stimulus current in Amperes
V_dut = peak stimulus voltage in Volts
Xc = impedance in Ohms

Note that the expected V_dut is a peak value that needs to be multiplied by 2 when measured with Pk-Pk measure type.

For example:

For a 1nF capacitor the impedance when measured with AC2 is

$$Xc = \frac{1}{10000 \cdot 1nF} = 100K\Omega$$

$$Istim = \frac{100mV}{100K\Omega} = 1uA(peak)$$

Longhand Test Properties page

The longhand Test Properties page should then be setup as follows:

- Stim: 1 uA AC2
- Measure: (100mv * 2) ± tol, measure type Pk-Pk

```
18xx Windows mode-init_com
Edit  Options  Tools  Save  Revert  Validate  Quit
Component Properties  [ ↑ ]-[ ↓ ]

Test Properties  [ ↑ ]-[ ↓ ]
Options              Indicators          Current Page
 Pre  Post  Cntrl                          Page 1 of 1
Test Type: Test V Stim I    Extended: Off
Test Data
Scale    : mv     Stim Value (ma) : 1     Stimulus      : Pin 1 (42)
High     : 220    Scale           : ua    Measure       : Pin 2 (68)
Low      : 180    Stim Type       : AC 2  Reference     :
Measure Type : Pk-Pk                      Wait (ms)     : 0
                                          Squelch (ms)  : 0
Controls
Wire Mode: 3    Precise: Off    Highguard:  Off    Averaging: 1
Guard Mode: Active
Fast Mode: Off

C:/TPD/KMAR1 - ICT            START  CANCEL  SOF  HLD  RPT  CRT
```

Wait times. Be aware that wait times need to be kept short when you test capacitors in longhand mode. Long wait times can adversely affect the result.

Since longhand tests are not specific to the component under test, the system cannot correct for errors and parasitic values that makes longhand tests less precise than shorthand test for the same component.

Conversion. To automatically convert a shorthand test into a longhand test, use the Convert to Longhand selection from the Tools pull-down menu while Test Properties for a particular shorthand capacitor is displayed.

		AC1	**AC2**	**AC3**			**AC1**	**AC2**	**AC3**
10	PF	1.00E+08Ω	1E+07Ω	1.00E+06Ω	10	NF	100000.00Ω	10000.00Ω	1000.00Ω
18	PF	5.56E+07	5.56E+06	5.56E+05	18	NF	55555.56	5555.56	555.56
22	PF	4.55E+07	4.55E+06	4.55E+05	22	NF	45454.55	4545.45	454.55
27	PF	3.70E+07	3.70E+06	3.70E+05	27	NF	37037.04	3703.70	370.37
33	PF	3.03E+07	3.03E+06	3.03E+05	33	NF	30303.03	3030.30	303.03
39	PF	2.56E+07	2.56E+06	2.56E+05	39	NF	25641.03	2564.10	256.41
47	PF	2.13E+07	2.13E+06	2.13E+05	47	NF	21276.60	2127.66	212.77
56	PF	1.79E+07	1.79E+06	1.79E+05	56	NF	17857.14	1785.71	178.57
68	PF	1.47E+07	1.47E+06	1.47E+05	68	NF	14705.88	1470.59	147.06
82	PF	1.22E+07	1.22E+06	1.22E+05	82	NF	12195.12	1219.51	121.95
100	PF	1.00E+07	1000000	100000	100	NF	10000.00	1000.00	100.00
180	PF	5.56E+06	5.56E+05	55555.56	180	NF	5555.56	555.56	55.56
220	PF	4.55E+06	4.55E+05	45454.55	220	NF	4545.45	454.55	45.45
270	PF	3.70E+06	3.70E+05	37037.04	270	NF	3703.70	370.37	37.04
330	PF	3.03E+06	3.03E+05	30303.03	330	NF	3030.30	303.03	30.30
390	PF	2.56E+06	2.56E+05	25641.03	390	NF	2564.10	256.41	25.64
470	PF	2.13E+06	2.13E+05	21276.60	470	NF	2127.66	212.77	21.28
560	PF	1.79E+06	1.79E+05	17857.14	560	NF	1785.71	178.57	17.86
680	PF	1.47E+06	1.47E+05	14705.88	680	NF	1470.59	147.06	14.71
820	PF	1.22E+06	1.22E+05	12195.12	820	NF	1219.51	121.95	12.20
1	NF	1.00E+06	100000	10000.00	1	UF	1000.00	100.00	10.00
1.8	NF	5.56E+05	55555.56	5555.56	1.8	UF	555.56	55.56	5.56
2.2	NF	4.55E+05	45454.55	4545.45	2.2	UF	454.55	45.45	4.55
2.7	NF	3.70E+05	37037.04	3703.70	2.7	UF	370.37	37.04	3.70
3.3	NF	3.03E+05	30303.03	3030.30	3.3	UF	303.03	30.30	3.03
3.9	NF	2.56E+05	25641.03	2564.10	3.9	UF	256.41	25.64	2.56
4.7	NF	2.13E+05	21276.60	2127.66	4.7	UF	212.77	21.28	2.13
5.6	NF	1.79E+05	17857.14	1785.71	5.6	UF	178.57	17.86	1.79
6.8	NF	1.47E+05	14705.88	1470.59	6.8	UF	147.06	14.71	1.47
8.2	NF	1.22E+05	12195.12	1219.51	8.2	UF	121.95	12.20	1.22

4 DIGITAL DEVICES

If you have an analog-only test system, information regarding digital test is not pertinent to your test situation. The analog-only functionality prevents you from generating, editing, or running digital tests.

Gray Code and Vector Overview

Generally, a digital IC test applies logic signals to a device's inputs and analyzes the signals that appear on the outputs. The applied logic signals are either Gray code stimuli or vectors. The results of the Gray code stimuli on the outputs are analyzed (measured) with three possible digital measurement methods: CRC, Count, and High. The results of the vector pattern stimuli are measured by a comparison to known-good patterns.

Gray code frequencies are effective digital stimuli for testing

- SSI and MSI devices
- PALs where test patterns are unavailable
- RAMs and ROMs, all addresses are generated and all cells checked
- some LSI devices where the need for programming is limited

Using Gray code to test a device with large numbers of inputs becomes difficult because Gray code has only 14 unique stimuli.

Vector patterns are effective for complex pattern sets where no regular or coherent stimulus patterns exist, and for sampling digital responses where each bit is individually compared to known-good data. Tester-per-pin architecture provides a unique driver behind every pin, thereby allowing stimulus by random patterns.

Vectors are effective digital stimuli and response patterns for testing PALs, ASICs, LSI, VLSI, and boundary scan devices.

Digital Test Properties for Gray code and vector tests, explained later in this section, provide fields to specify the digital stimulus and measurement requirements.

Refer to the **Z1800-Series Programmer's Guidebook**, Chapter 5, for information about guards and disables and for further background information regarding digital test philosophy.

Digital Test Specifications

Non-Multiplexed Stimulus

Every pin has a unique driver zand receiver.

- Every driver is capable of providing both Gray code and vector stimulus
- Fixed +5 Volt Driver Reference

  V_{oh}(max) = +4.5V, no load

  V_{oh} = +3.0V, I_{oh} = 350 mA

  V_{ol}(min) = +0.2V, no load

  V_{ol}= +0.8V, I_{ol} = 200 mA
- Slew Rate:

  120V/us, no load

  100V/us, 90 ohm load

  150v/us, Rise, 1 Kohm || 100 pF

  160v/us, Fall, 1 Kohm || 100 pF

Programmable Measurement Threshold Reference

- Threshold reference can be programmed -2 V to +9.95 V. Accuracy of programming is 1% ±35 mV.
- Can select comparison to dual or single threshold.
- Programmed threshold levels and type (dual or single) apply to all measurements in a test step.

Driver/Receiver Boards—Digital Measurement

Driver/receiver boards are organized for digital measurement in two sections, each section having a 16:3 matrix.

Programming features of the boards are as follows:

- Threshold comparison at driver/receiver board
- Receiver Specs:

Threshold detection accuracy: Threshold reference ± 200 mV

The receiver will transition from one state to the other if the input signal is more than 200 mV from the threshold reference cited above. For example, if receiver output is logic low and the threshold reference is 1.0 V, receiver output will go to logic high when the input signal exceeds 1.2 V.

- Acceptable voltage range going into the receiver without damaging the tester:

  -10V to +10V, response only pin

  0V to +5V, stim and response pin
- Open receiver input defaults to Logic High Input Resistance:

  4 Kohm, minimum
- Single threshold, digital only tests:

  Minimum 3 measurements/burst

  Maximum 6 measurements/burst
- Dual threshold, digital only tests:

  Maximum 3 measurements/burst
- Mixed mode: analog measurement reduces possible digital measurements by one for the burst in which analog measurement is taken.
- Mixed mode: analog stimulus reduces possible digital measurements by one for all measurements in group.
- Software automatically assigns measurement pins to matrix, no special fixture wiring required.

Termination Resistors

- Provide loads to measurement nodes
- Choices: 1K and 500 Ohms to +5V, Prog 5.5 V, or ground, or 1K each to +5 V, Prog 5.5 V, or ground
- Adds ~500 pF to measurement node when selected
- Default: No terminators selected

Software Features

- Software can automatically learn response from DUT
- Software Timeout: The software timeout notifies the user if a burst will exceed user-specified backdrive timeout and will not run the burst. Default: No timeout

Duty Cycle Control

- Allows user to specify maximum duty cycle of backdrive in a test program.
- Default = 0 (Run at maximum speed, no enforced cool-off)
- Percent specified = backdrive time/off-time & backdrive time

Gray Code Tests

Refer to the table below for a description of Gray code's significant characteristics.

Property	Description
Clock ticks	All generators clocked from a common source, and move in lockstep with one another, producing identical stimulus timing relationships each time a burst runs.
Common timing origin	All edges related to timing origin, one clock tick before first edge of F1.
No simultaneous transitions	At each clock tick, one and only one stimulus channel changes state. Thus small timing-skew changes from pin to pin cannot significantly affect test results (no-race conditions). Also, since signals are static most of the time, and one signal changes at a time, crosstalk and noise are minimal.
Double coverage bursts	A burst of F1, F2, and F3 signals would (in the default case) terminate at the rising edge of F5, having twice attained each of the 8 possible states.
Repeatable logic path	Ensures that each board receives the same, repeatable test.
Easily visible markers	For triggering oscilloscopes or logic analyzers while debugging. (Test window and measurement window.)

Specifications

Measurement types:

- Signature Analysis (CRC) up to 2 MHz

  Hicheck, if selected, identifies stuck high pins.
- Transition Counting (COUNT) up to 5 MHz
- Duty Cycle (HIGH) up to 2 MHz
- One COUNT or HIGH measurement per burst
- COUNT and HIGH always run in separate bursts.

Measurement enable timing:

- Specified per measurement pin
- All pins in a burst have same enable timing
- Programmed in reference to Gray code frequencies:

  FROM—Specifies when measurements begin, Default F1.

  TO—Specifies when burst ends, Default: F(N+2),where FN is highest stimulus frequency programmed.

  WHILE—Allows specifying up to 2 frequencies that must be true in order for measurements to be enabled.

  Default—always

Pattern Depth: 1 k pin memory

Device Size Constraints:

- Disables: 128 nodes maximum
- Device pins in test: 128 maximum
- Guards per test: 20 maximum

Programmable clock rate

- Clock Frequency = 2MHz/CD, where CD= Clock Divisor) 1 <= CD <= 200
- Default and Maximum Frequency: 2MHz (CD =1)
- Minimum Frequency: 10 KHz (CD = 200)
- Single clock for stim and measure

Hardware time-out: <= 16 ms @ 2 MHz

Hardware timeout is at F16 <= 16 ms @ 2 MHz. It increases proportionately with the changing clock divisor. For example, when CD = 2, timeout is 32 ms.

Mixed mode: Analog stimulus and measurement within digital test.

- Up to 10 analog pins per test step (device)
- Single analog stimulus in each group
- Single analog measurement per burst
- Software ensures that analog measurement falls within digital burst

Gray Code Stimulus

Up to 14 Gray code frequencies (F1 through F14) and their complements (F1* through F14*), preset high (PH), preset low (PL), preset pulse (PP), logic high (LH), and logic low (LL) can be applied to the device-under-test in any combination. Preset pulse works only in conjunction with the programmed frequency. Connect and disconnect features also provide synchronous three-state function.

Typically, clock pins use the higher frequencies such as F1 and F2. Major mode controls use the lower frequencies, such as F13 and F14. Address and data pins use the middle frequencies. The signatures you receive will depend on the IC functionality and stimulus assignment. Remember that the measurement window can change with changes in the stimulus.

Stimulus	Frequency*	Period*	Data Rate	1st Transition*
F1 + F2 + F3 ...+F14	1 MHz	1 µs	2 Mbit/sec	0 µs
F1	500 kHz	2 µs	1 Mbit/sec	0 µs
F2	250 kHz	4 µs	500 kbit/sec	0.5 µs
F3	125 kHz	8 µs	250 kbit/sec	1.5 µs
F4	62.5 kHz	16 µs	125 kbit/sec	3.5 µs
F5	31.25 kHz	32 µs	62.5 kbit/sec	7.5 µs
F6	15.63 kHz	64 µs	31.25 kbit/sec	15.5 µs
F7	7.8125 kHz	128 µs	15.63 kbit/sec	31.5 µs
F8	3.90625 kHz	256 µs	7,812.5 bit/sec	63.5 µs
F9	1.95313 kHz	512 µs	3,906.25 bit/sec	127.5 µs
F10	976.56 Hz	1.024 ms	1,953.13 bit/sec	255.5 µs
F11	488.28 Hz	2.048 ms	976.56 bit/sec	511.5 µs
F12	244.14 Hz	4.096 ms	488.28 bit/sec	1.023 ms
F13	122.07 Hz	8.192 ms	244.14 bit/sec	2.047 ms
F14	61.04 Hz	16.384 ms	122.07 bit/sec	4.095 ms
F15**	30.52 Hz	32.768 ms	Non-stim	8.191 ms
F16**	15.26 Hz	65.536 ms	Non-stim	16.384 ms

*Clock divisor 1
**F15, F16 are available for measurement timing only.

There are 32 basic stimulus types available:

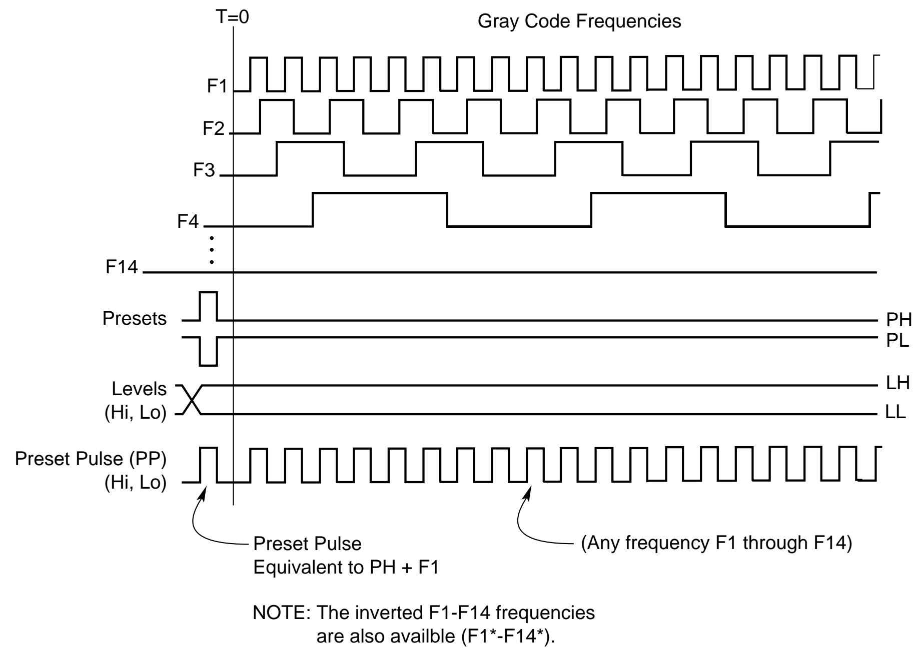
- 14 Gray codes F1 through F14
- 14 Gray code complements F1 through F14 (F1*, etc.)
- preset high
- preset low
- logic high
- logic low

In addition, frequencies can be grouped: F1 + F3 + F5.

The frequencies are bit stream inputs. The highest Gray code frequency is F1 (500 kHz at clock divisor = 1), the lowest, F14. Each frequency (F*n*) is one-half the lower frequency (Fn-1), where n is an integer 1 through 14. Each higher frequency (in terms of F number) is half the frequency of the preceding one. Note that only one frequency changes state at any given clock time. All Gray code stimuli terminate at the end of the execution burst.

The following illustration shows the 32 basic discrete Gray code inputs.

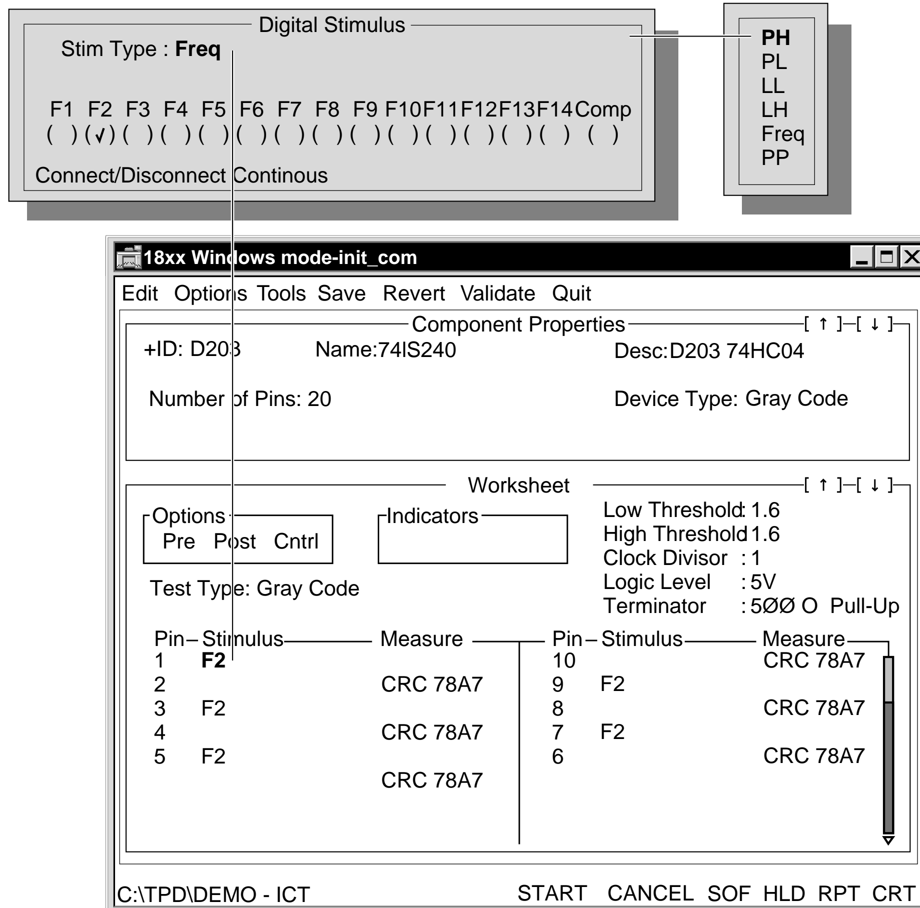
Gray-code digital waveforms (32 in all, including complements)



Each of the tester’s channels has its own individual Gray-code generator. The generators are powerful, flexible, and easily programmed. The signature generators, which evaluate the behavior of ICs on the DUT, measure during an interval known as the listen window. Selected edges corresponding to the Gray-code set open, close, and gate the listen window.

You can use Gray code in debug mode to validate that stimuli are stable by checking that a change in each input pin’s stimulus also changes at least one of the output signatures. Also, the signature should not change when you change the clock rate.

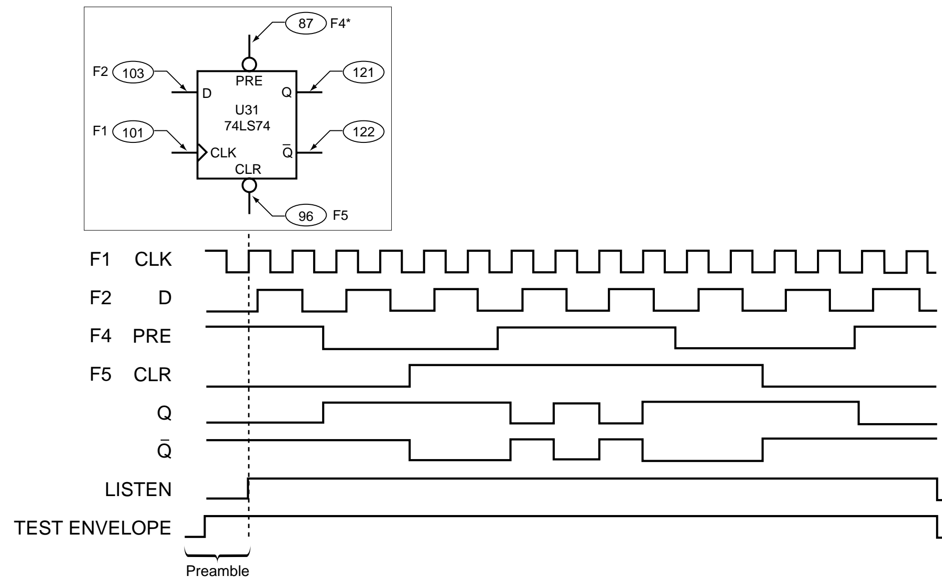
When you edit the Stim Type and Stimulus Frequencies in the Digital Stimulus window, you will affect the overall measurement window timing. It is important to note, however, that if you change the Stimulus Type from Freq to another type such as LL or PH, the measurement timing will remain the same unless you deselect any frequencies enabled in the Stimulus Frequencies area before changing the Stim Type.



Stimulus Example

In the following illustration of an MSI test, a set of Gray code digital stimuli is applied to the flip-flop's various inputs. The highest frequency, F1, is assigned to the CLK input. The lower frequencies F4* and F5 are assigned to the asynchronous inputs, Preset and Clear, respectively.

MSI testing—D-type flip-flop example.



The resultant signature at the Q output would be unique to that stimulus pattern. You may similarly assign F4 and F7, and so on.

An intermediate frequency such as F2 or F3 is assigned to the D input. The Q output is sampled at each clock tick and processed by the signature generation circuit to produce a four-character hexadecimal value, in this case F443. The Q* output signature for this example is 09AD.

Gray Code Measurement

Measurement Types

Three measurement types are available for making Gray code digital measurements: CRC, COUNT, and HIGH.

Cyclic Redundancy Check. The CRC, or Cyclic Redundancy Check, measurement type is the most precise, and therefore the preferred of the three measurement methods. It should be used in situations where the device-under-test can be initialized to a known beginning state. If the device can be initialized, then as long as a controlled stimulus is applied and the measurement circuits are synchronized with the stimulus, the device outputs will produce a consistent and repeatable response.

The CRC measurement type analyzes response data over a specified period of time (the listen window) and divides the data by a set polynomial ($X^1 + X^{12} + X^5 + 1$) to produce a remainder in the form of a four bit hexadecimal signature. Each output data stream generates a unique signature or CRC. Any change in input produces a different CRC for the outputs. A CRC can also be affected by a tri- state condition in the measurement window or an output which may have a relatively slow rise time.

Measurements on tri-stated outputs should be avoided, or if unavoidable, a pull-up or pull down should be programmed to ensure that the measured output always tri-states to the same state. Open collector devices may have slow rise times if they are heavily loaded or if they have a weak pull-up. Clock these tests down or program an additional pull-up to ensure a stable CRC. Up to six CRC measurements can be made per digital burst. The actual number depends on:

- wiring configuration
- Hicheck usage
- group considerations
- threshold types
- mixed mode usage
- differences in the listen window

Count. The Count measurement type counts the number of positive-going transitions through the programmed threshold during the measurement window and displays them as a five-digit decimal number. The maximum display for the count function is 65535 which corresponds to 6.5535 MHz. The Count clock is 8 MHz, so measuring frequencies above 5 MHz is not practicable. Counting more than 65535 transitions in one window will result in counter circuit overflow. Counting 65537 transitions will display a count of 00002 or two counts beyond 65535. Multiple simultaneous Count measurements are not possible because the THC or VP contains only one count circuit. The count measurement method is useful when the device-under-test cannot be initialized and the beginning state of the device is unknown. Since the Count measurement type is used on devices that cannot be initialized, a measurement range rather than a single value should be programmed. The TO range specifier in the Digital Measure window is provided for this purpose. Free-running clocks and counters are prime examples of devices which will need the count measurement type.

High. The High measurement type counts the number of master clock pulses that occur while the measurement node is at a logic high state. The result is displayed as a five-digit decimal number with an upper limit of 32767 (2 MHz master clock counted out to F16 or for 16.384 ms). Multiple simultaneous High measurements are not possible for the same reasons as the Count measurement type. The high measurement type is useful when the device cannot be initialized or if the duty cycle of the device is the desired measurement parameter. One-shots are prime examples of devices which are best tested with the High measurement type. Using Clock Divisor multiples of two on a High measurement will result in measurement data that directly corresponds to the device time-out. Use master clock frequencies of 1MHz (Clock 2) or 100KHz (Clock 20) or 10KHz (Clock 200) for direct measurement data correlation.

Measurement Windows

Care should be taken when programming FROM, TO, WHILE 1, WHILE 2 parameters. Unexpected measurement windows may be generated if invalid arguments are chosen.

Whenever Gray code stimuli are programmed, and a node is measured using one of the above measurements types, the system software creates a default measurement window. The default measurement window starts just after the first transition of F1 and ends just before the first transition of the frequency, which is two frequencies beyond the highest numbered frequency programmed. For example, if the highest stimulus frequency used is F4, the default measurement window begins on the first transition of F1 and ends just before the first transition of F6. The default measurement window can be modified to start and stop at selected intervals and further modified to make measurements only at selected times within the selected start and stop points.

The Digital Measure parameters that accomplish these modifications are:

- From
- To
- While 1
- While 2

FROM. The FROM measurement modifier indicates where the measurement window should open. Valid arguments to the From parameter are F1 through F15. Choosing FROM: F8 in the Digital Measure window would program a digital measurement window that starts just after F8 goes high and ends just before F10 goes high. The FROM parameter is useful when the device-under-test requires time to reach a known state. Shift registers that cannot be initialized and outputs that have very slow rise times are prime examples of devices that need the FROM measurement modifier.

TO. The TO measurement modifier indicates where the measurement window should end. Valid arguments to the TO parameter are F2 through F16. Choosing TO: F8 in the Digital Measure window would program a digital measurement window that starts just after F1 goes high and ends just before F8 goes high.

WHILE 1. The WHILE 1 measurement modifier indicates that measurements should only be made while the programmed frequency is true within the FROM TO range window. Valid arguments to the From parameter are F1 through F14. The compliments of these arguments are also available. Choosing While 1: F5 in the Digital Measure window would program a digital measurement window that starts just after the programmed FROM point and samples only while F5 is high until just before the programmed TO point goes high.

WHILE 2. The WHILE 2 measurement modifier is an extension to the WHILE 1 modifier. It adds a second while parameter to the programmed From-To window. Choosing WHILE 2: F7 Comp (V) to the above While 1 example would create a Listen window that sampled only while F5 was high and F7 was low.

Using Gray Code to Test Memory Devices

Memory tests using Gray code stimulus and signature analysis methods provide 100% pin-level fault coverage for most devices.Gray code is engineered in such a way that if you assign a different frequency to each input, when you measure a device to the default measurement window, you automatically realize all the input states for that device.

Use a group of Gray code frequencies to produce all possible address combinations on the address bus inputs of ROMs, for example. Gray codes or static levels provide the necessary control input signals, like chip select and output enable. A CRC (signature) type of measurement on each data output pin collects the long streams of output data. The CRC for each data output pin uniquely represents the exact data pattern that results from the Gray code stimulus patterns applied at the device input pins.

An SRAM test can also employ Gray code frequencies to write data into the device before reading out its contents. Generally, a frequency lower than those on the address lines operates the Read/Write* line. The lower-numbered frequency covers the entire address space while writing a data pattern into the SRAM. The Read/Write* line transitions before the same addressing reads back the contents. The Read/Write* line's stimulus frequency can also control the measurement interval (window) and sample only the read data.

Unlike SRAM tests, DRAM tests require refresh operations (RAS/CAS cycles). To achieve the RAS/CAS operation, use two Gray code frequencies to generate the two signals. The most common arrangement is to use an inverted F1 (F1*) for CAS and F2 for RAS. These frequencies provide the most common RAS/CAS relationship where the RAS signal goes low, CAS goes low then high, and RAS returns high. If RAS and CAS are F1 and F2, the address bus must be a lower (high-numbered) frequency.

Vector Tests

Vector stimulus allows specifying drive high, drive low, or high impedance state for each pin and for each clock cycle.

Vector measurement allows specifying expect high, expect low, or ignore for each pin and for each clock cycle.

Specifications

Measurement enable timing

- Vector Enable specifies each pin at each clock cycle independently.
- Global Ignore specifies that all measure pins are ignored on a given clock cycle.

Pattern Depth:

- Vector Processor board contains 1 Mbyte VP1, or 4 Mbyte VP3, of memory, with 64K reserved for use by its microprocessor.
- Remaining memory is available for test patterns.
- Memory consumption is pattern-dependent.
- Each clock cycle consumes at least 4 bytes.
- No maximum pattern depth is enforced, and 100K patterns (clock cycles) should be achievable.

Device Size Constraints:

- No device size constraints are enforced, other than those of tester hardware:

  Maximum nodes = 2048 for 1820, 1860, 1890, and 1888-2

  = 640 for 1800, 1840, 1880, and 1888-1
- Disable nodes:

  Quantity limited only by tester hardware. Duplicate nodes produce an error message.

  Disables can be any series of vectors, and are applied prior to the patterns specified in the digital Test Properties.

  Both Gray code and vector disables are run before all digital tests. The order in which they are run depends on the type of test you are executing. Refer also to the **Z1800-Series Programmer's Guidebook**, Chapter 5.

  Disable nodes hold their last state during the test page burst.
- Guard nodes:

  Quantity limited only by tester hardware.

  Guard nodes are specified as additional nodes in the digital Test Properties portion of the Step Worksheet.

Programmable clock rate

- Separate clocks for stimulus and measurement.
- The stimulus clock reference is free-running.
- The period of the stimulus clock reference is programmable for each test step.

  Programming resolution: 25 ns

  Clock Divisor (CD): 20 <= CD <= 32767

  Default and minimum period: 500 ns (CD=20)
- Multiple stimulus clock reference periods may elapse between stimulus clocks (i.e. the stimulus clock period is irregular, but synchronous to the reference).
- All stimulus pin changes are synchronous with the stimulus clock.

- For a test step, all measurements are taken the same amount of time after the stimulus clock.
- The measurement delay is programmable.

  Programming resolution: 25 ns

  Measurement Delay (MD): 4 <= MD <= CD

  Default period: 500 ns (MD=20)

  Minimum period: 100 ns (MD=4)

  Measurement delay cannot exceed stimulus clock reference period.

Vector Test Methods

Z1800-series testers with the Vector Performance option are capable of performing vector tests on digital devices. While Gray code testing allows for easy-to-understand and easy-to-create programs, vector testing provides great flexibility in specifying the test pattern. A vector test pattern specifies the state of each stimulus pin and the expected state of each response pin for every clock cycle of the pattern. Since each pin is uniquely specified, its pattern is completely independent from the other pins. Whereas Gray code test patterns are predictable and repetitive, vector test patterns can vary greatly, from extremely repetitive, like a clock pin, to completely random, like a serial data stream. Devices such as microprocessors and programmable peripheral devices have read and write cycles that cannot readily be created with Gray code, but are easily managed with vector test patterns.

Vector testing is useful not only because it is flexible, but also because its usage is so prevalent. Custom devices such as ASICs are typically tested by vector test patterns. These patterns can be translated into a format that the Z1800-series testers can use, allowing board test a step up in creating a test for those devices. Similarly, programmable devices such as PALs frequently have JEDEC format test vectors. The Z1800-series can take in these patterns for use in board test.

Vector Processor Controller Board

The Vector Performance option is required on Z1800-series testers in order to test digital devices using vectors. The heart of the Vector Performance option is the Vector Processor controller board (VP). The VP employs a unique patented approach in performing vector tests. The VP approach maximizes memory efficiency. The efficiency is realized in several ways. First, memory is centralized. All memory resides on the VP controller; there is no pin memory. Vectors of great length can be created since lengths are not constrained by per pin memory. Until all memory is used up, more vectors can be stored. Next, the memories store pin transitions, rather than actual pin states, thus reducing the amount of memory required to store a vector. Finally, memory is reused. Each clock cycle has a set of pins associated with it. The set of pins is stored in a list. The list is stored only once, but multiple clocks (states) can use it.

The VP is very efficient at applying deep vector patterns. The VP supports vector test using the same driver/receiver boards used in a standard Z1800-series tester for Gray code tests and requires no special fixture considerations. Its capacity for long vectors supports Boundary Scan and deep memory testing.

Vector Clock—Priming Pins

When running a digital test burst, the VP accesses its centralized memory and uses that data to address and prime pins one at a time. Priming notifies a pin that is about to change state. After priming all pins, the VP issues the vector clock, causing all primed pins to change state and clearing all primes. One effect of serially addressing pins is that the pattern changes at irregular intervals. If many pins must change on a clock cycle, all of those pins must be addressed individually and primed for change. Priming applies to both stimulus and measurement pins. Priming of a measurement pin indicates a change in expected data. The architecture is well suited for testing static gate arrays and other devices insensitive to clock rate.

The vector clock is synchronized to a master clock (default frequency is 2 MHz) and is issued only after all active pins are primed. The vector clock always occurs at a master clock edge, but consecutive vector clocks may occur after multiple master clocks. The time required to prime all pins is proportional to the number of pins changing state. The more pins that change state, the longer it takes to prime them, resulting in irregular clock intervals. The VP can prime up to two pins within the 500 ns (default) clock period. Each additional prime takes 150 ns with additional time added as needed for synchronization to the master clock. Most test patterns change a few pins on each clock cycle, and infrequently change many pins (usually an address or data bus), so that the pattern rate will average out about 1 MHz (half the default clock rate).

Digital Response Signals

Z1800-series testers support six simultaneous digital measurements. Digital response signals travel from the driver/receiver boards to the controller board through six digital response lines. The controller captures and processes the digital response signals.

On the VP controller, each digital response line has a prime circuit like that on the driver/receiver board. For vector tests, expected responses are stored in memory, along with the stimuli. Transitions in the expected response are primed like stimulus nodes and change state on the stimulus clock.

The tester has only six digital response lines, but can have as many as 2048 pins. A vector test can expect data on all 2048 pins, at least in theory. All vector tests that require more than six digital measurements run multiple bursts automatically in order to capture all of the results. For each vector test burst, a map memory assigns response pins to the six digital response lines.

Map Memory

Each location in the map memory corresponds to a unique tester pin. Since the tester can have 2048 pins, the map memory has 2048 locations. The data stored in each map memory location determines if the corresponding pin is active for the present burst, and if active, the digital response line on which the pin data is expected. If a response pin is active, then the expected response for the appropriate digital line is primed. If a response pin is inactive, then no primes occur.

The contents of the central memory used for priming memory remain constant for all bursts of a given vector test; only the map memory is modified for each burst. Two advantages result from this. First, since the list never changes, each burst of the vector has identical timing. This makes test results repeatable. Next, map memory modification is much simpler and quicker than modifying expect data within the central memory. Reloading the map memory takes at most twelve write operations: six to clear old assignments, and six to set new assignments. Reloading central memory would take many calculations, and could involve thousands of memory write operations. In addition to modifying map memory, response relays are set and cleared between bursts. The time to write the map memory is small compared to relay settling.

Behavior of Disables

When running multiple burst vector tests, the entire stimulus pattern, including disables and guards, runs for each and every burst. Both vector and Gray code disables will hold state after their disable sequence runs, and until the end of the test pattern burst. For example, if the last state of a vector disable sequence programmed the pin high, the pin will remain high through the test pattern burst. For a Gray code disable, logic high, logic low, and presets will act as expected. If a disable frequency is programmed, it will act as a logic low for a true frequency, and as a logic high for a complemented frequency.

Be aware that the Disable Table Test Properties function checks for duplicate nodes in vector and Gray code disable tables. An error message opens if a duplicate node is entered.

Refer to the **Z1800-Series Programmer's Guide**, Chapter 5, for more information about Gray code and vectors.

VP Stimulus and Measurement Clocks

When using the Z1800-series test head controller (Gray code only), stimulus and response use the same clock. The response from one cycle is recorded at the clock for the next cycle. With an irregular vector clock, test results could be erratic with a single clock. With the VP controller, measurement capture uses a second clock. The stimulus clock toggles all primed stimulus pins and expected responses. The measurement clock captures the resulting response. For a given test, the measurement clock issues a fixed time after the stimulus clock. This keeps the delay from stimulus to measurement constant throughout test, in spite of the irregular stimulus clock rate.

The stimulus clock triggers the measurement delay countdown, producing a measurement clock with a programmable delay relative to the stimulus clock. The minimum measurement delay is 100 ns and is programmable in 25 ns increments. The measurement clock for one cycle must occur at or before the next stimulus clock.

Failure Register

Vector tests compare actual and expected response at the measurement clock edge, and store the result in memory and in a global response failure register. The global response failure register has a failure flag for each digital response line. The failure flag for a response line sets whenever the line fails and stays set throughout the burst. This allows the software to quickly determine failing pins because it does not have to read the entire response memory. The software retrieves the response memory contents when displaying results for tests debug and when learning the response.

Programming the Listen Window

The listen window for a response pin can be programmed in two different ways. The first is to program the individual expect-high, expect-low, and don't care for the pin for every state. The other method is to use Global Ignore. Global Ignore acts as a don't care for all response pins for clock cycles in which it is programmed. Global Ignore eliminates the need to prime each response pin into a don't care state. This is especially useful when dealing with buses that pass through an unknown state. The transitions can all be ignored, and then only the pins whose final state changed need to be primed. Refer to the **Z1800-Series Programmer's Guidebook**, Chapter 11, for more information.

Pole Assignments for Vector Tests

Homing Loops and Mixed Mode with Vectors make the pole assignment for vector tests complex. In tests with homing loops, it is possible to construct a test which cannot execute due to a lack of available measurement poles.

All nodes in the 1800-series systems have access to six measurement poles, named E_d, F_d, G_d, E_s, F_s, and G_s. The d stands for drive and the *s* for sense, for historical reasons related to the poles used to perform analog Kelvin (that is, four-wire) measurements. For this reason, if a test has more than six measurement pins, it must be broken up into multiple bursts. All stimulus pins must, of course, be active during each burst.

Each driver/receiver board in the test head cage serves 32 nodes; the lower 16 nodes can directly access the three drive poles, and the upper 16 have direct access to the three sense poles. In addition, there are three bridging relays which can connect any drive pole to the corresponding sense pole (for example, the F_d pole to the F_s pole). As a result, all nodes have potential access to all poles. The benefit of this bridging capability is that it often allows more measurements per burst than would otherwise be possible. For example, without bridging, a test having measurements on nodes 0, 1, 2, 32, 33, and 34 would require two bursts, each using all the drive poles. However, with bridging, all six nodes can be put into one burst; nodes 0, 1, and 2 on the

drive poles and nodes 32, 33, and 34 bridged to the sense poles. Note that nodes can be bridged only if the pole being bridged to is not being used by another node on the same driver/receiver board.

Dual thresholds also limit the number of nodes that can be measured in a burst. When a dual threshold measure is specified, two complementary poles (for example, G_d and G_s) are assigned to the measured node and the bridging relay between them is closed. Thus, no more than three such measurements are possible in a burst.

Analog stimuli and measures affect how poles are assigned to the vector measurement nodes. Only one analog stimulus is allowed; it is always assigned to the E_d pole and must be present in all bursts. Ten analog measures are allowed (nine if there is an analog stim), and they are assigned to the F_d pole, one per burst.

Finally, there are Homing Loops pins whose corresponding measurement nodes, like analog stimuli, must be included in every burst. There is no limit, however, to the number of pins which can be specified as homing loop pins. As a consequence, it is possible to construct a test which cannot meet all of the above requirements. For example, a test with an analog stimulus, and two homing loop pins, all within the same 16 node group on a driver/receiver board would be unable to measure any of the remaining 13 nodes within that node group. If a situation such as this occurs, an error message will be displayed (if run from the vector editor), which states that no poles are available to execute this test. You will have to take appropriate action to reduce the demand for poles.

Digital Test Editing

You may edit a digital disable or component test step at any time from the Step Worksheet.

To access a digital Step Worksheet from the Main menu, select:

1. The board program
2. Edit
3. Digital
4. Disables or Components (If you select Disables, then choose GC_DIS or VEC_DIS.)
5. the digital Step Worksheet from the Component Select window (only for components).

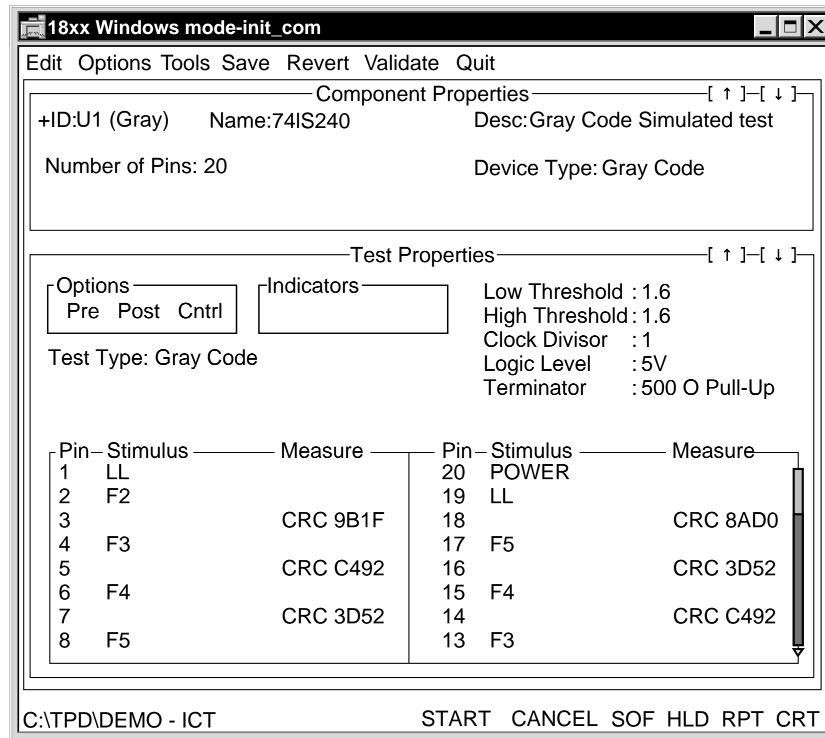
The Step Worksheet contains a menu bar, Component Properties, and Test Properties.

Refer to the **Z1800-Series Programmer's Guide**, Chapter 3, for an explanation of digital Component Properties.

Digital Test Properties areas (Gray code and vectors) contain the execution data for a single test step.

Gray Code Test Properties

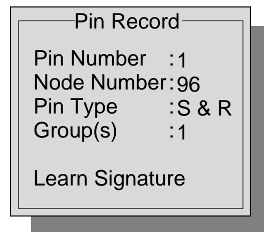
Like analog Test Properties, Gray code Test Properties have a single page which appears in its entirety when you select a Gray code test. The following illustration shows a typical Gray code Step Worksheet.



Refer to the following table for Gray code Test Properties field details.

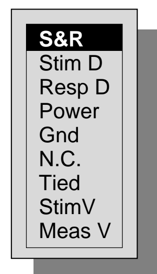
Field	Description
Indicators	Shows if there are Gray code and/or vector guards. Read only.
Low Threshold	Range of -2 to +9.95 Volts. Default is 1.6.
High Threshold	Range of -2 to +9.95 Volts. Default is 1.6.
Clock Divisor	Governs the clock rate during bursts. The default of 1 provides a 2 MHz master clock; clock divisor 2= 1 MHz; clock divisor 4=500 kHz, and so on.
Terminator	Resistive load applied to measurement, usually required for open-collector outputs and for verifying the enable of 3-state devices. Choices are: 1K pull-up, 500 Ohm pull-up, 1K pulldown, 500 Ohm pulldown, None, and 1K terminator. Pull-ups are to +5V and pull downs to ground. The 1K terminator has 1K to +5V and 1K to ground.
Logic Level	Specifies whether your device is 3 volts or 5 volts. The default is 5 V.
Pin	Device pin number. Select to edit Pin Record Menu.
Stimulus	Stimulus applied to the device's inputs. Select field to select one of the following: PH, PL, LL, LH, Freq, and PP.
Measure	The expected response data for the applicable device output pin. Select from: Measure Type: CRC, COUNT, HIGH Value 1, Range: OR, Single, TO Value 2 From, To, While 1 and 2

The Pin column lists all the device pins. When you select a Pin field, the Pin Record appears.



Pin Number is a number of the device package's pin. Node Number is the tester's node number. Pin Type lists possible pin functions. Group(s) represent digital burst groupings.

A group is a subset of nodes on an IC package used to test one logical element, such as a single NAND gate in a quadruple NAND gate package. Typically, a group describes all inputs and outputs of a single element. A pin can be assigned to a single group or to multiple groups.



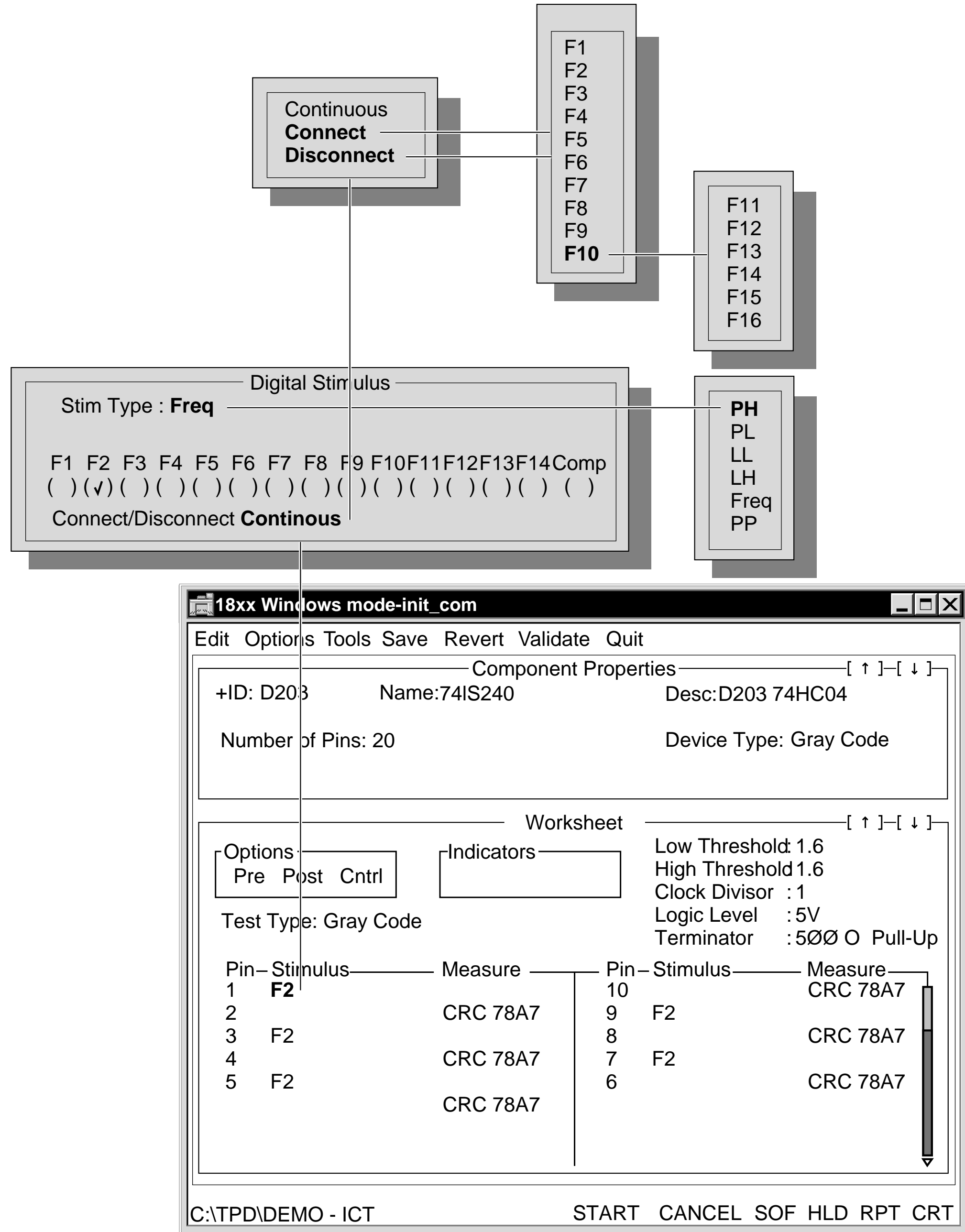
Pin Type offers the pop-up window at left from which you may choose a function for the pin. S&R represents digital stimulus and response. Stim D is digital stimulus only. Resp D is digital response only. Power and Gnd are labels for pins tied to power (logic high) and ground (logic low) sources. NC representsa no pin connection. Tied means that the pin is tied to another signal pin. Stim V (Test Digital Stim Voltage) and Meas V (Test Voltage

Stim Digital) are for mixed mode testing.

Refer to the end of the Digital Test section for further discussion of mixed mode testing.

The Stimulus field allows you to select one of the following stimuli for the corresponding pin: PH (pulse high), PL (pulse low), LH (logic high), LL (logic low), PP (preset pulse), Freq (Gray code frequencies F1 to F14 and their complements, also for PP.)

Select the Stimulus field to view the Digital Stimulus window.

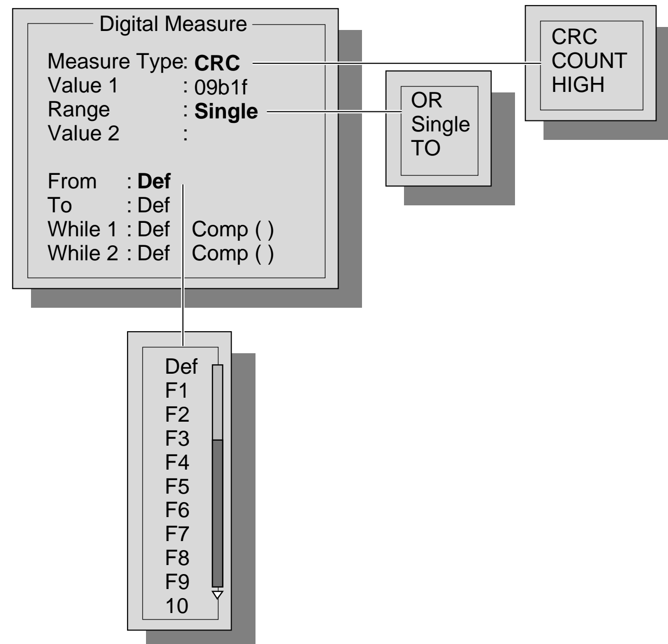


The Comp field inverts all selected Gray code frequencies for that pin. In other words, you may not select F3 and the complement of F5 at the same time. You cannot select the complement of logic levels and pulses.

Multiple frequencies produce the Exclusive-Or of the individual frequencies. Select the Comp field to obtain the inverted signal.

The Connect/Disconnect field allows you to select one of 16 frequencies. Continuous indicates a continuous, uninterrupted frequency burst. Connect activates the stimulus only during the times the qualifier is in the high state. For example, F1 Connect F10 applies F1 when F10 is high. Disconnect disables the stimulus only during the times the qualifier is in the high state. For example, F1 Disconnect F10 disables F1 when F10 is high.

The Measure field allows you to select Measure Type, Value 1, Range, Value 2, and From, To, While 1 and 2 with complements. To access the Digital Measure window where you can make these selections, click the Measure field. Within the Digital Measure window the Measure Type, Range, and From, To, While1 and While2 fields expand as shown below.

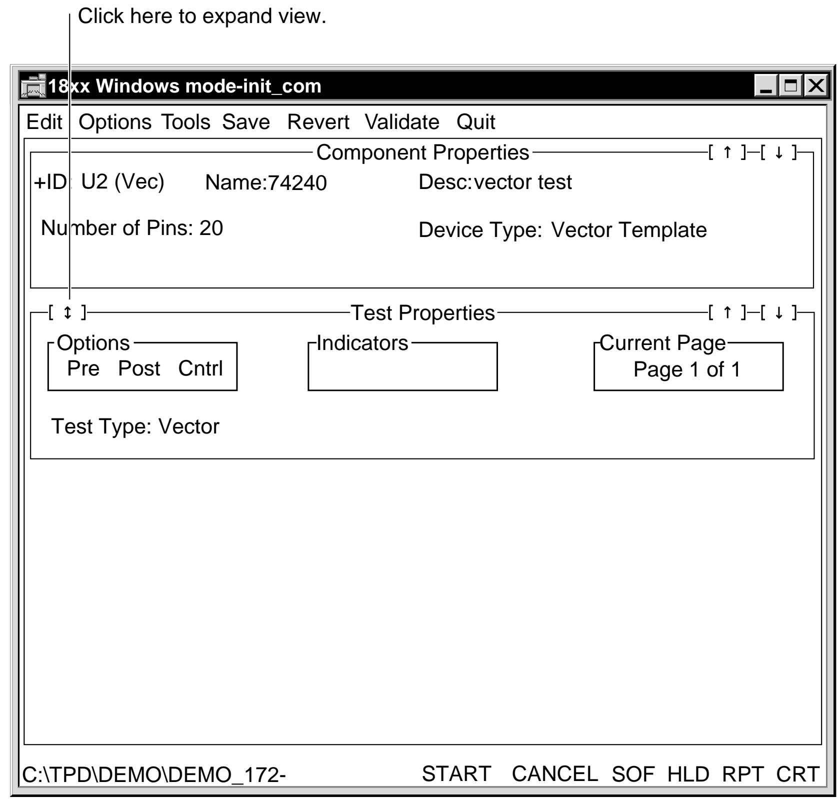


Selecting OR or TO from the Range field enables the Value 2 field.

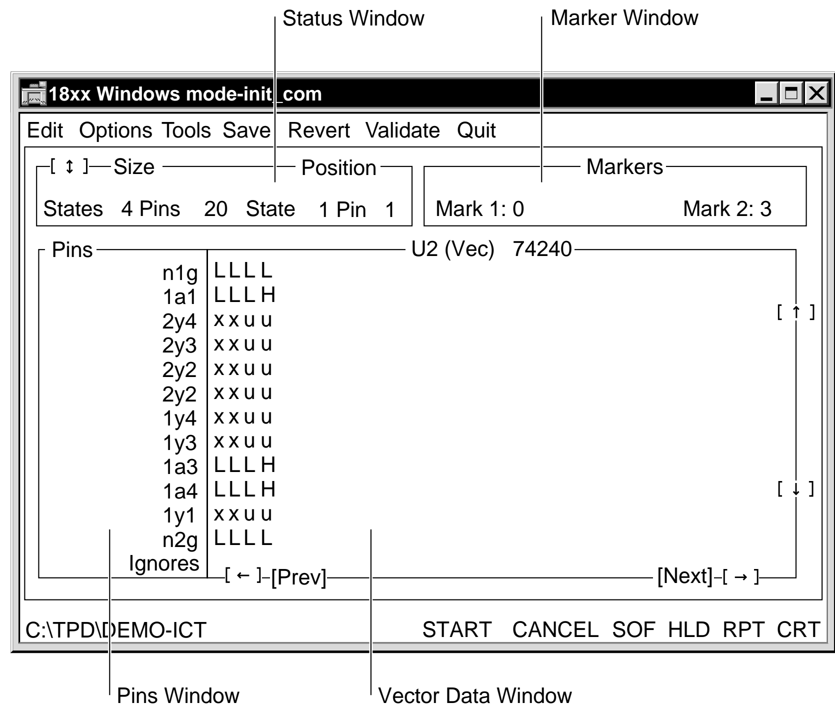
When you click a From, To, While1 or While2 field, the frequency scroll window appears. Use the scroll bar to access F11 through F16. Select the Comp field to select the inverted signal.

Vector Test Properties

When you first access a vector test, a Step Worksheet similar to the following appears.



When you click the double-pointed arrow, the Test Properties page expands as follows:



The Vector Editor is made up of four windows. They are the Status Window, Marker Window, Pins Window, and Vector Data Window. Movement between these windows can be accomplished with the mouse or the F2 key which changes windows in a counterclockwise order.

Revert. Select Revert at any time to go back to the Test Properties variables last saved on disk.

Status Window

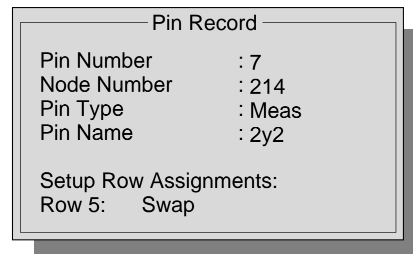
This window contains the overall dimensions of the vector and the current cursor position in the Vector Data Window. To go to a particular position in the Vector Data Window you can enter the coordinates in the State and Pin fields and either press Enter or click the mouse. The double-arrow field when clicked or Entered will take you back to the compacted Test Properties page.

Markers

Markers are vertical bars within the Vector Data window. They are there to mark a particular pattern for easy reference. Two markers are supplied. As default these markers come up at the first and last pattern of the vector. To move a marker, just enter the pattern number in one of the marker fields and press Enter or click. To go to a marker position double-click one of the marker fields and the Vector Data window will reposition at that marker if it is not already visible. An alternate way to move markers is to click and hold the mouse button down on the border of the Vector Data window directly above a marker. The marker bar will disappear. With the mouse button still down, drag the mouse to the position that you would like to place the marker and release the button. The marker will appear at that position.

Pins Window

The pin names for each row of the Vector Data window are listed here as well as a row for Ignores. This window scrolls vertically with the movement of the Vector Data window. Also the Up, Down, and Enter keys can scroll the Pins window if pressed at the top/bottom of the window. This window's scrolling is tied with the Vector Data window—if one scrolls vertically, so does the other.



Clicking or pressing the keypad's plus key on a field in this window presents the Pin Record window.

Pin Type allows you to specify Unused, Stim, Meas, Stim/Meas, Monitor, Stim V, Meas V, Homing Meas, or Homing S/M.

Pin Name is a 9-character text field for the name of the pin.

With Setup Row Assignments, pins can be moved vertically in the vector editor using the Row and Swap/Insert fields. Initially the row will display the current row of the vector editor that this pin resides in. By entering a different number in this field you can change the row of this pin in the display. Swap will make this pin trade rows with the pin specified in the row field and Insert will put this pin in the row specified and push all the pins below it down one. This feature is useful for putting all the pins of a data bus side-by-side on the display.

If a pin type is one in which a response will be taken—Meas, Stim/Meas, Monitor, Homing Loop Meas, Homing Loop Stim/Meas, Mixed Mode Meas— then other fields will be present in the Pin Record Menu window.

- Assigned Pole
- Trigger
- Learn Expect Data

The Assigned Pole field indicates the actual measurement pole that has been assigned to a pin so that you know where to place your probe on the test jack panel when the Trigger function is On.

The Trigger field enables you to toggle the Trigger function On and Off. When On, only the vector burst containing this pin will generate a test envelope at the test jack panel. Selecting a pin automatically deselects any other pin.

Refer to the **Z1800-Series Programmer's Guide**, Chapter 11, for more information about using it to debug vector tests.

The Learn Expect Data field is for learning the measured responses. When you click or press Enter on this field, the data in the Vector Data window for this pin will be replaced with the measured data. This function takes place on a per pin basis—you can learn only one pin at a time. Furthermore, Learn Expect Data is limited to processing 32K of failures in any one pass. If there is more than 32K's worth of failures on one pin, you must select Learn again to learn all of the data associated with that pin.

Vector Data Window

The Vector Data window allows you to examine and manipulate the data patterns of the vector. You can move in this window by paging or scrolling. Paging moves the window by one half of its width/height, scrolling moves the window by one line. To page vertically use the up and down arrows in the left border or press the Page Up and Page Down keys. To page horizontally, use the left and right arrows in the bottom border or use the key combinations of Ctrl-Left Arrow and Ctrl-Right Arrow. To scroll, use the left, right, up, and down arrow keys within the Vector Data window.

You can toggle the state (H, L, Z, u, d, x) of an individual cell within the vector data window by clicking the cell or using the Space bar. See the table below for an explanation of the default state characters. You can modify the character set by selecting Modify/Data Characters from the menu bar. A query window will allow you to edit either hexadecimal or ASCII characters.

State	Description
H	Drive High
L	Drive Low
Z	Tristate
u	Sense Up
d	Sense Down
x	Ignore

If you are working with bidirectional pins, there is no Z state. Because Z and x states are the same on Stim/Meas pins, the software allows you to create only an x state on such pins.

The software system cannot instruct you on the best method to correct a bad vector, but it can simplify the process by disclosing failed or unexpected data. When you select Start to run the test step, the software translates, loads, and executes the vector table. If the burst does not pass, failures will be highlighted with a defined fail color. The NEXT function lets you advance to the next failing state. The PREV function lets you return to the previous failing state. When you depress the mouse button on Prev or Next, the cursor highlights the failing vector data cell. When you release the mouse button, the cursor control returns to either Prev or Next. Holding the mouse button down keeps advancing to the next (or previous) failure.

With the RPT (repeat) function, you can determine if results are stable over a large number of repetitions. The delay function allows you to move a sampling strobe with respect to the vector clock signal. With the Learn Expect Data function, you can import test results into a test program and discard the previously programmed results. You are not required to enter any of these results—the software will do the work. Note, however, the software will change only those states which are specified as u or d; it ignores changes to the ignore state.

With SOF (Stop On Fail), you can run a program as an operator. If you choose the editor, the cursor will indicate the first failing bit.

Edit. The Edit command places the cursor in the Vector Data window at the position specified by State/Pin in the Status window.

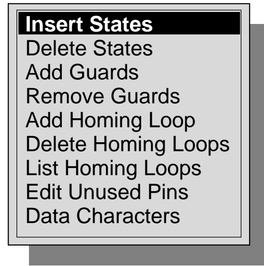
Save. The Save command briefly issues a message that it is saving the vector test step.

Compress. The Compress command builds a new, compressed internal image of the vector in the form of pointers and lists, and reloads the new pointers and lists into vector processor memory. Editing of vectors creates lists in the vector file that are not referenced any more. Executing Compress after editing will remove these unreferenced lists and run the list sharing algorithm to get maximum use of the list space. Vector compression is not necessary for proper test execution, but when performed, reduces RAM and disk space storage requirements.

When you select Compress, two brief process messages appear.

If you have a slow PC, large vector files will require more time for compression.

Modify. The Modify command allows you to change vector states, guards, pins, homing loops, and strings and to automatically ignore failing states.



Insert States. Insert States allows you to pad out the overall vector by adding additional patterns. The result will be a vector with more states, useful, for example, when additional clock cycles are necessary at a particular point in the test vector. Insert States copies the vector state only immediately prior to insert; it doesn't give an alternating pattern on the inserted states. You must edit them in.

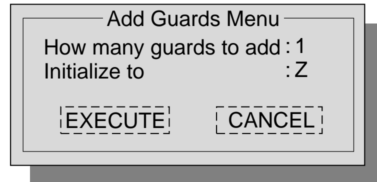
If new states are being added, a window (Insert States Menu) appears asking at what state the addition should start and how many states are being added.

Execute the Insert States menu by entering states and selecting Execute.

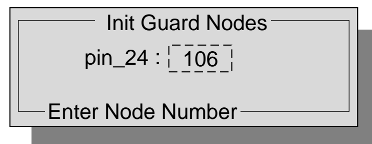
Cancel aborts the window. The software adds the new, states in the edit fields after issuing process messages.

Delete States. Delete States works in much the same way as Insert States, except that it deletes rather than inserts the specified number of test vector states.

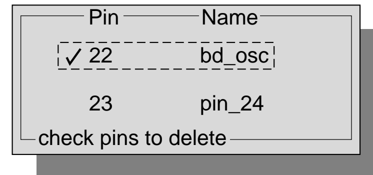
Add Guards. Add Guards allows you to add new guard pins. Guard pins isolate the device from surrounding devices on the board. The Add Guard window appears.



After you select Execute to add the guard or guards, the software will issue process messages, then prompt you to assign a node number or numbers into the window below. Press Enter to complete the process.



Remove Guards. Remove Guards allows you to remove the pins and associated signal names from the vector edit window. A deletion window similar to the one below appears when you select Remove Guards.



Click or press the Space bar on an item to mark the pin/name for deletion. Press the Enter key when done.

A query window will ask you to confirm deletion. Select Yes to remove the guard. The software will then issue process messages and remove the marked guard or guards.

Homing Loops

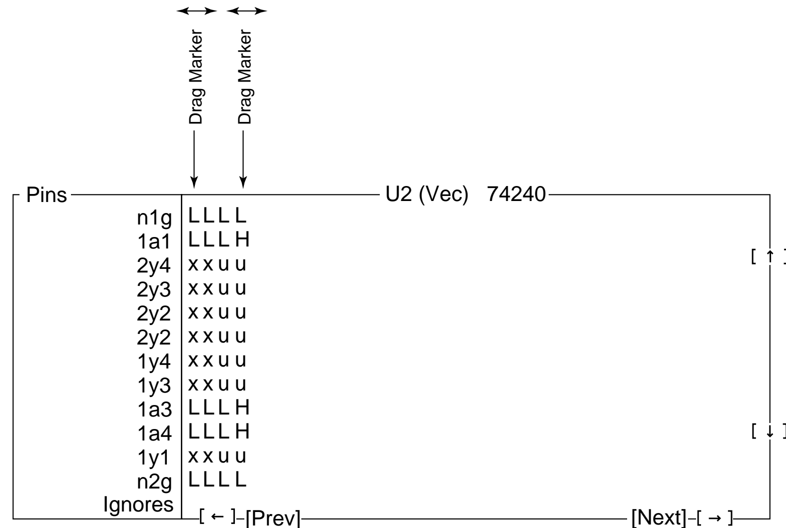
Homing loops extend board test coverage to include devices that do not have a master reset pin or command to initialize them to a known state. The homing loop function allows initialization of the device before each section is tested.

To implement the function use the vector editor Modify menu to add, delete and list the homing loops.

Add Homing Loop. To add a homing loop to your test program

1. Select the desired vector test from the Component Select window.
2. Click the double-pointed arrow in the left portion of Test Properties to expand the page, invoking the vector editor window.

3 Define the range for the homing loop by dragging the vertical markers to the start and end states of the desired homing loop, or by entering the desired column numbers in the Markers subwindow at the upper left of the screen.



4 Select Modify/Add Homing Loop.

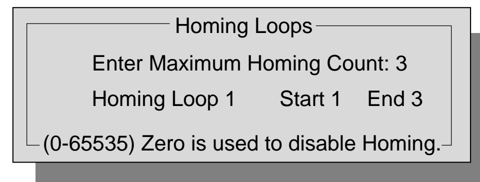
A query window appears asking you to select OK to create a homing loop that is defined by the area between the two markers. You may also select Cancel.

Homing loops cannot overlap. If Add Homing Loop is selected when the markers either overlap or surround existing homing loops, then the homing loops that intersect with the newly defined homing loop will be deleted, and the homing loop defined by the markers will be added. This feature can be used to modify existing homing loops simply by repositioning the markers and selecting Add Homing Loops. When you have selected the range of the homing loop, the area between the markers changes color.

You may select up to 10 homing loops per test.

5 Click OK in the next query window to save your edits.

A Homing Loop window similar to the one below appears.

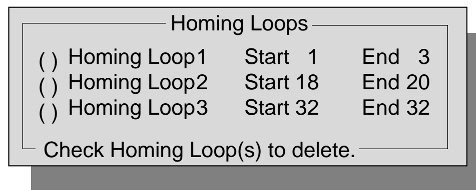


6 Enter the maximum number of times you want to execute the homing loop before aborting the test.

Delete Homing Loops. To delete homing loops,

1 Select Delete Homing Loops from the Modify menu.

A window appears listing the homing loops you have set up.



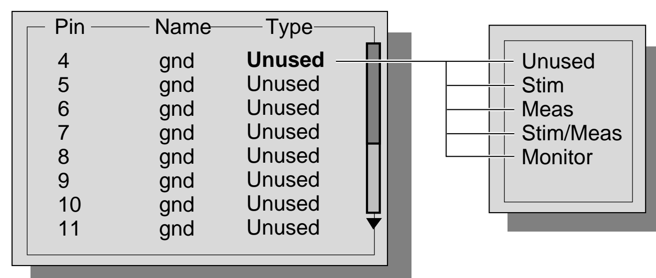
2 Click within the parentheses of the homing loop(s) you wish to delete.

The homing loops are deleted when you exit the window.

List Homing Loops. To list homing loops, select List Homing Loops from the Modify menu. A list of your selections appears on the screen.

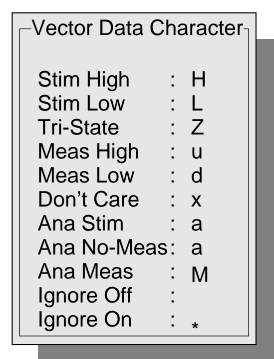
Edit Unused Pin. Edit Unused Pin allows you to assign an active pin type to an unused vector pin. (An unnecessary pin can be marked unused in the pin record. The unused pins are listed in the Edit Unused Pin window.)

Select Edit Unused Pin to view and edit the unused pins.



Select the Type field and choose one of the pin types. Select an area outside the window. The software will include the former unused pin in the vector edit window when it redraws the screen.

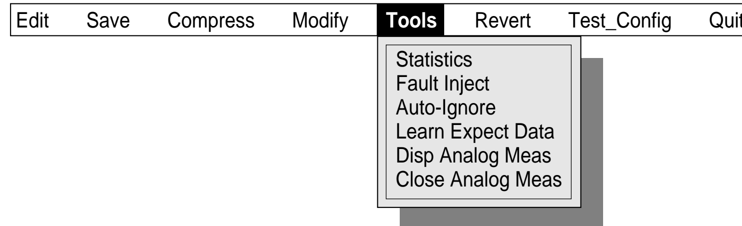
Data Characters. Data Characters allows you to select the data characters that represent the vector states.



Type your choices into the fields of the Vector Data Character window. The characters shown in the window are the default characters (ASCII). You can select either HEX or ASCII characters. The software will issue an error when you enter an unauthorized character.

Tools

The Tools menu provides access to the Statistics window, Fault Inject function, the Display Analog Measure and Close Analog Measure functions.



Statistics. The Statistics command allows you to produce a statistical report of the vector test. The report will appear on the screen in a window similar to a program output window. To control window scrolling and cursor movement, refer to quick help (F1) for instructions.

The report contains information about pin activity on a pin-per-pin basis. The report displays the State number of the first toggle and the number of toggles for each pin with regard to both stimulus and measurement.

More than one toggle on a particular pin does NOT necessarily mean that the pin has achieved both possible data states.

If in the State of First Toggle column for either Stim or Meas there is a field of asterisks ********, then this pin had no toggles, that is, it is not being tested. This can be used as a quick reference to identify test coverage of your vector.

The statistics window can be closed by either clicking outside the window or pressing ESC. A window will appear asking if you would like to save this report to a file.

A vector test statistical report will look similar to the one below.

			State of First Toggle		Number of Toggles	
Pin	Name	Type	Stim	Meas	Stim	Meas
1	clk	I	0	-	100	-
2	r22	I	3	-	8	-
3	lpor	I	3	-	9	-
4	gnd	U	-	-	-	-

Press ESC to Quit

Fault Inject. Fault Inject is a tool to help you assess the quality of a digital test by analyzing test patterns for failing output when any one input or bidirectional pin is held to a constant high or low state. In other words, you should expect to see failing test results when you inject a fault on a pin. If there are no failures, then the test is not a good test to detect the fault injected. Fault Inject is intended for use on passing tests so that if there are any failures, they can be attributed to the injected fault.

The Fault Inject interface consists of the Fault Inject window listing all the pins you are allowed to include in the Fault Inject analysis, their types, and names. You can specify whether you want to hold/analyze the pin high, low or both high and low.

When you execute Fault Inject, a report window appears showing the fault coverage and detailed results.

Refer to the **Z1800-Series Programmer's Guide**, Chapter 11, for detailed information about using Fault Inject.

Auto-Ignore. Auto-Ignore allows you to change all failing states of a vector test to the don't care (X) state. The feature is most useful when a vector test generated by the program generator has timing problems. Auto-Ignore automatically changes U and D states to X when the edges from the template cannot be met by the tester.

To use this tool

1 Select Auto-Ignore from the Modify menu.

A window appears prompting you for a range of pins and vectors to ignore.

Auto-Ignore

Auto-Ignore Range is From: 0 To: 3

	Pin	Type	Name		Pin	Type	Name
( )	0	Stim/Meas	n1g	( )	16	Stim/Meas	2a4
( )	1	Stim/Meas	1a1	( )	18	Meas	n2g
( )	14	Meas	2a3				

Select All Clear All Execute Cancel

Enter State to Start Auto-Ignore at

2 Specify the range of states.

By default, this range is all of the patterns of the vector. If you want to narrow that range, enter that range in the Auto-Ignore Range field.

3 Select the pins which you wish to have the test mark as ignored.

Either click Select All to specify that you want all failures ignored, or click within the parentheses to select particular measure or stimulus/measure pins. If you click Select All, you can deselect individual pins by clicking the check marks within the parentheses.

4 Click Execute to confirm your selections and execute the test or Cancel to terminate the procedure.

Learn Expect Data. The Learn Expect Data field is for learning the measured responses. When you click or press Enter on this field, the data in the Vector Data window for this pin will be replaced with the measured data. This function takes place on a per pin basis—you can learn only one pin at a time. Furthermore, Learn Expect Data is limited to processing 32K of failures in any one pass. If there is more than 32K's worth of failures on one pin, you must select Learn again to learn all of the data associated with that pin.

Display Analog Measure. The Disp Analog Meas field is for monitoring the test set up and monitor the test as it runs When you select Tools/Display Analog Meas the following window appears.

Pin	Node	Burst	State	High	Meas	Low	Scale	Status
3	210	65	1	5.000	0.000	4.000	V	Pass

You can drag the window to the bottom of the screen to monitor the results as the test runs.

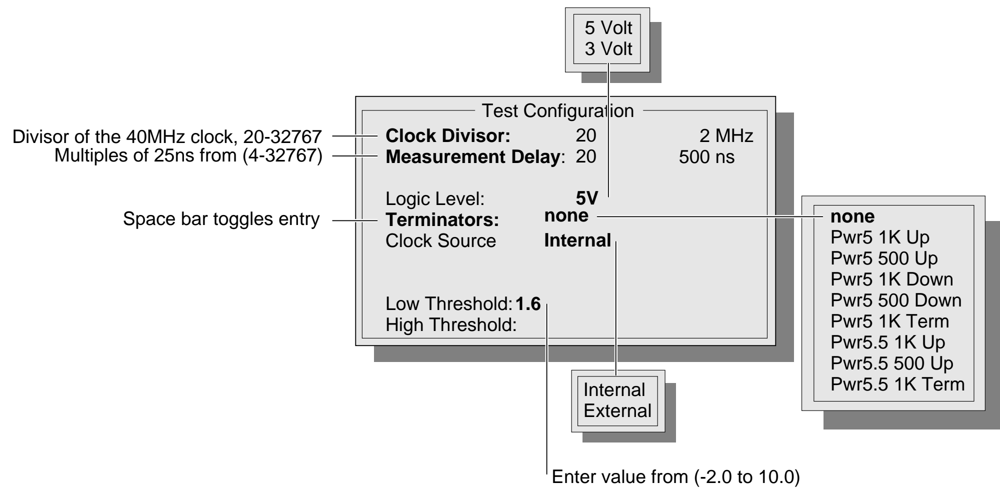
Close Analog Measure. Select Close Analog Meas when you want to remove the Display Analog Measure window from the screen.

Test_Config. Test_Config allows you to check the current status of the following digital test control features.

Refer to the following table for a complete description of Test_Config fields.

Field	Description
Clock Divisor	Sets maximum frequency rate of pattern application. Internal master clock=40 MHz, therefore a divisor of 20 yields pattern application rate of 2 MHz maximum. In a vector test, some patterns may be slower if a great number of changes occur on the next pattern in the vector. External Clock Sources are not affected. Range, 20–32767.
Measurement Delay	Sets the measurement strobe delay time relative to the stimulus clock (clock that triggers all pins to change from pattern to pattern). Units are expressed in 25 ns increments from the stim clock. 20 corresponds to 500 ns; 10 to 250 ns, and so on. If a specified measurement delay is longer than the time it takes for a pattern to execute, the measurement strobe is truncated by the next stim clock and occurs at that time. Truncation applies to Internal Clock Sources only and usually results in a stable measurement even though measurement occurs at the next stim clock. The user must ensure that the Measurement Delay is less than the clock period when an External Clock Source is used. Range, 4–32767.
Logic Level	Specifies whether your device is 3 volts or 5 volts. The default is 5 V.
Terminators	Applies resistive load to measurement, usually required for open-collector outputs and for verifying the enable of 3-state devices. Choices are: None, Pwr5 1K Up, Pwr5 500 Up, Pwr5 1K Down, Pwr5 500 Down, Pwr5 1K Term, Pwr5.5 1K Up, Pwr5.5 500 Up, and Pwr5.5 1K Term.Pull-ups are to +5V and pull downs to ground. The 1K terminator has 1K to +5V and 1K to ground.
Clock Source	Extends test coverage to include on-board clocks that cannot be overdriven by the tester. Uses an external clock to generate stim clocks for vectors. The EXT SYNC signal is edge sensitive in this mode; the VP will time out if you try to run a vector that uses an external clock signal and there is no external clock signal. Default is Internal. Maximum frequency is 2 MHz.
Low Threshold	Range of -2 to +9.95 Volts. Default is 1.6.
High Threshold	Range of -2 to +9.95 Volts. Default is 1.6.

See the Test Configuration window.



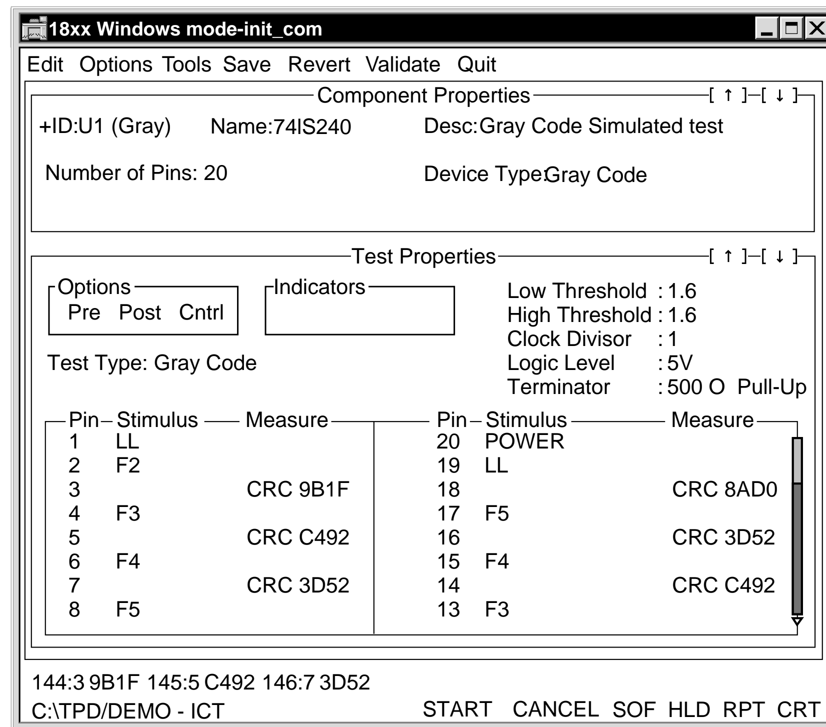
Mixed Mode Tests

A mixed mode test is a combination of a Gray code or vector test and a Linear test. You can have two types of mixed mode tests: mixed mode measure and mixed mode stimulus. A mixed mode test can have both mixed mode measure and stimulus within the same test. The following procedures show you how to develop each type.

Gray Code

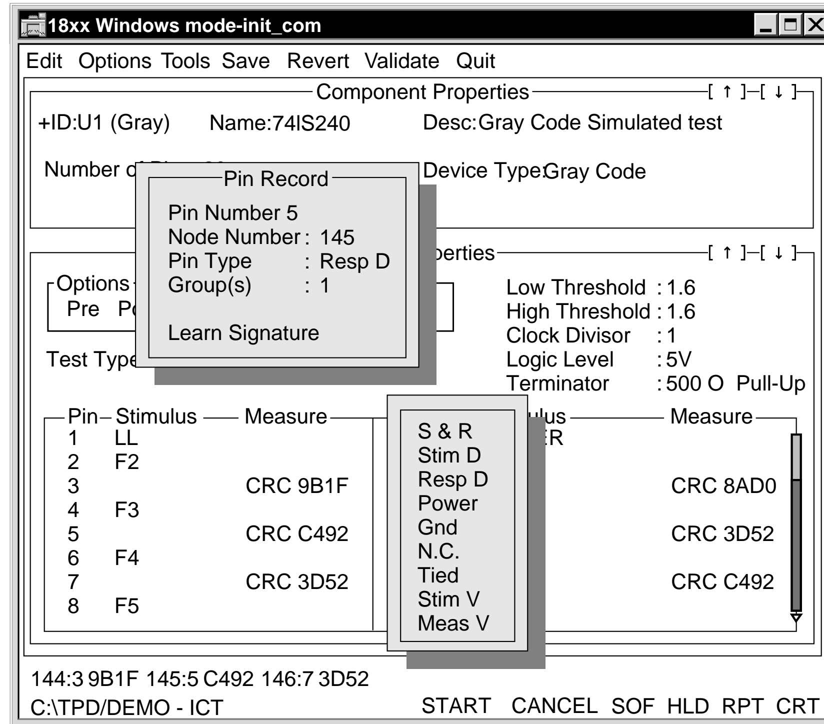
To add a mixed mode test to your program, you can modify a previously generated Gray code test.

1. Select Component from the Edit/Digital menu.
2. Select the desired Gray code test from the Component Select window.



(Note the items in boldface type. Values in the control line at the bottom of the screen will reflect changes made to pin 5.)

3 Click the number of the pin you wish to modify for a mixed mode test (in this example, Pin Number 5) to access the Pin Record.



4 Select Pin Type.

A pop-up box (shown in the center of the illustration above) appears enabling you to select, among other choices, Stim V or Meas V.

You can proceed to make your mixed mode test using either Stim V or Meas V. Both procedures are explained below, starting with Meas V.

Meas V Mixed Mode Test

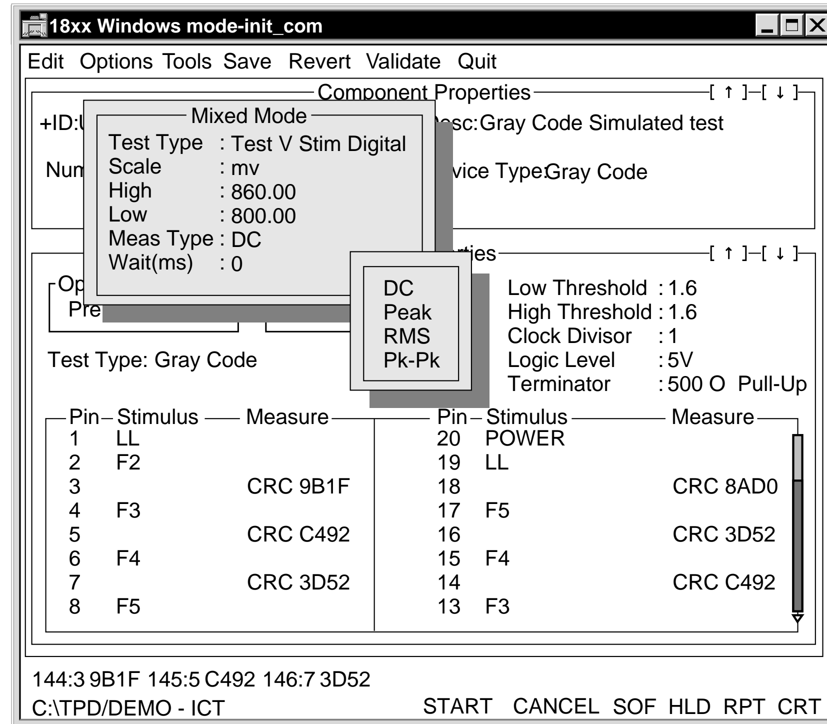
To change Gray code Test Properties and create a Meas V mixed mode test after you have performed steps 1–5 above

1 Select Meas V from the Pin Type pop-up box in Pin Record.

The Test Properties changes so that the measure field for pin 5 reads 0.00 V instead of CRC C492.

2 Click the measure field for pin 5.

The Mixed Mode pop-up window appears.



3 Click the Scale field and select the appropriate scale from the pop-up window.

4 Change the High and Low values as appropriate.

5 Click the Meas Type field and select the appropriate value, for purposes of this example, DC.

Refer to the Analog Measure section below for information about Wait.

6 Click outside of the Mixed Mode window.

Notice that the Measure field in Test Properties has changed. For example, in this case, to 860.00 mv.

7 Press Start to see the results of your changes.

Notice that the measure display line below Test Properties now shows an mv measurement rather than a CRC.

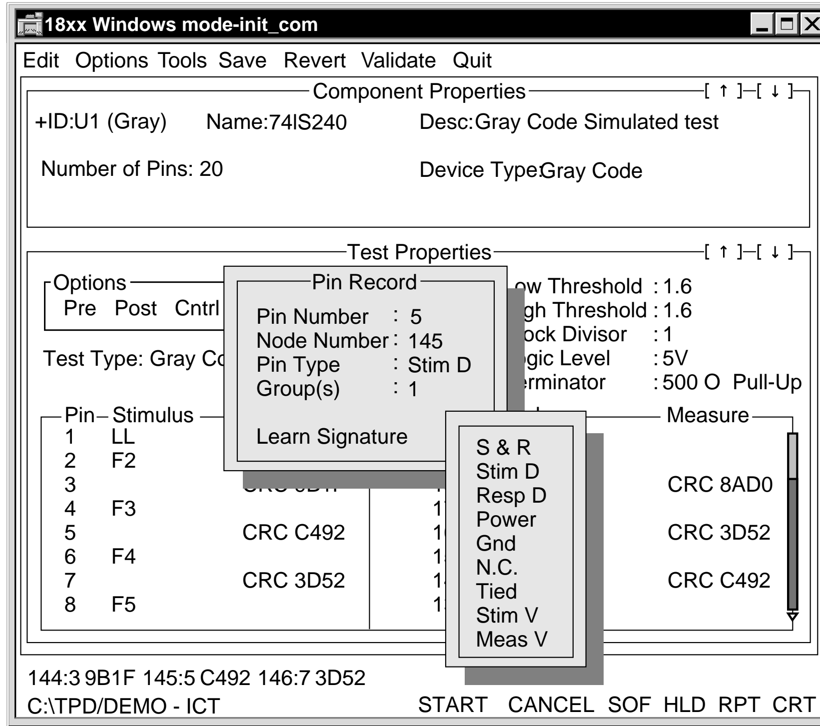
Stim V Mixed Mode Test

To change Gray code Test Properties in order to create a Stim V mixed mode test:

1 Perform steps 1-3 of Mixed Mode test.

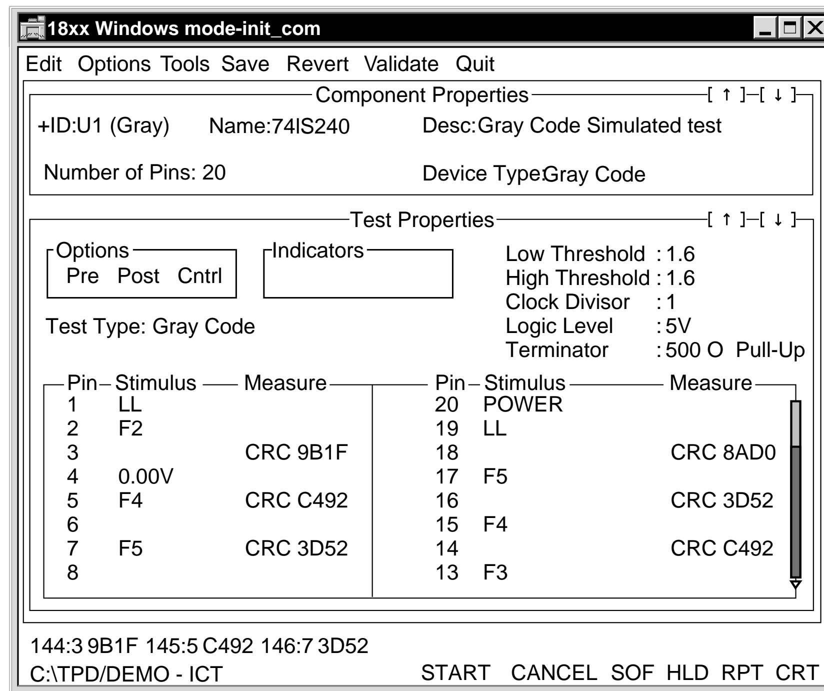
2 Click the number of the pin you wish to modify for a mixed mode test (in this example, Pin Number 4) to access the Pin Record Menu.

3 Select Stim V from the Pin Type pop-up box.



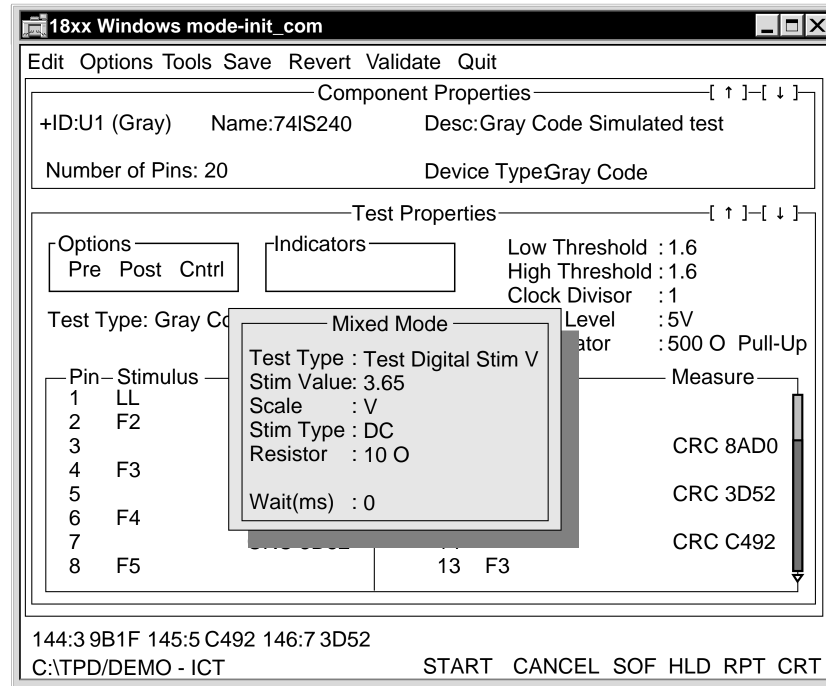
4 Click outside of the Pin Record Menu to return to Test Properties.

Notice that Test Properties changes so that the Stimulus field for pin 4 reads 0.00 V instead of F3.



5 Click the Stimulus field of pin 4.

The Mixed Mode window opens.



6 Highlight the Stim Value field and type in the appropriate value, in this case, for example, 3.65.

7 Click the Scale field and select the appropriate scale from the pop-up window, in this case for example, V.

8 Click the Stim Type field.

A pop-up window appears listing DC, AC 1, AC 2, AC 3.

9 Select the appropriate type, in this case, for example, DC.

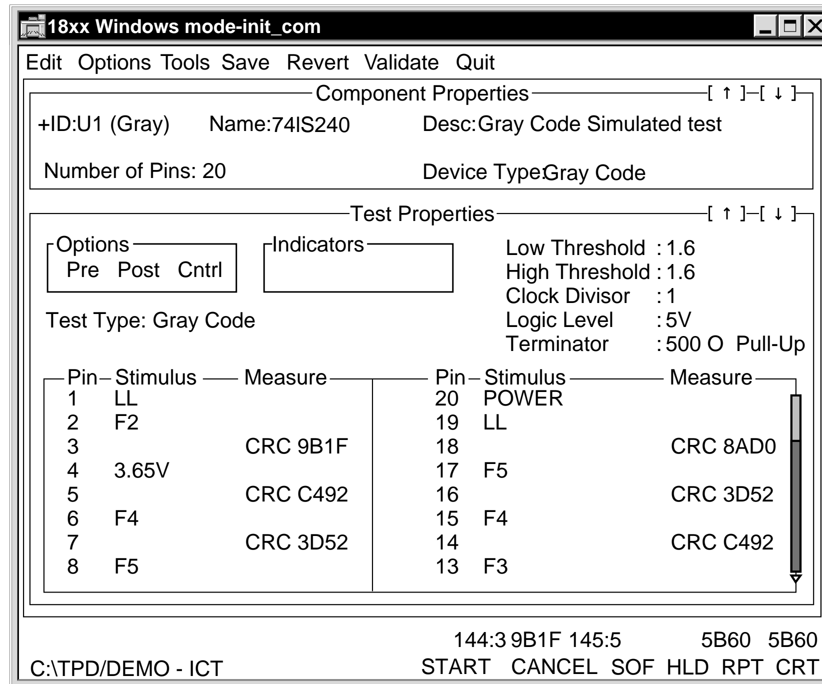
10 Click the Resistor field.

A pop-up window appears listing 0 O, 10 O, 100 O, 1 K, 10 K, 100 K, 1 M, 10 M.

11 Select the appropriate value, in this case, for example, 10 O.

See the Analog Measure section below for detailed information about Wait.

12 Press Start to see the results of your changes.



In the example above, agreement between the measure field for pin 5 and the CRC signature in the measurement display line indicates that you have created a valid test.

All analog measures are single-ended (the Reference node is not specified).

There can be only one analog stimulus per group. Stimuli can be in multiple groups as long as one group has only one analog stimulus. A group can have multiple analog measurements.

Analog measure wait time is the time from the start of the digital burst to the analog measurement. Analog measurement occurs while the digital stimuli are active. If the analog wait time is less than the duration of the current digital burst, the test is executed normally. If the analog measurement wait time exceeds the digital burst time, the software will equalize them by extending the To time of the digital test. If the analog measurement wait time is so long that the digital burst time cannot be adjusted in the To time, a warning message will appear. You can either modify the analog measurement wait time or the clock divisor.

In mixed mode, adding wait time may change the To time. This affects the digital measurement and require changing the expected CRC signature in Test Properties. Analog stimulus is applied before digital and holds throughout analog and digital measurements.

Vector Tests

As in Gray code tests you can have both mixed mode measure and mixed mode stimulus in vector tests. You can have both types in one test. You can have up to 10 measures in one test. If you have one stimulus, however, you can have only up to 9 measures. Only one analog measure per burst is allowed, and only one analog stimulus is allowed per test.

Meas V Mixed Mode Vector Test

To add a mixed mode test to your program you may modify a previously generated vector test.

Briefly, to add a mixed mode measure

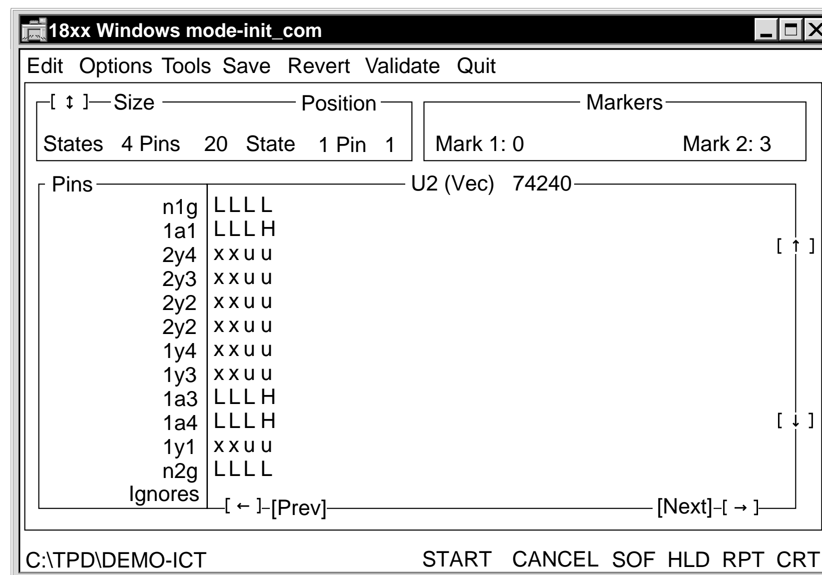
- Select the desired vector test
- Change the Pin Type.

When you are testing mixed analog digital devices such as D to A converters and A to D converters, it is possible to damage the test system's driver/receivers. To avoid possible damage, you must make sure that voltage at the node on the DUT never exceeds that node's drive high voltage, the voltage present at the V+ pin on the driver/receiver board. This rule applies only if the node is used in the test step as a digital pin type (Stim, Meas, Stim/Measure, Monitor). The rule does not apply if the pin type is Unused, Meas V, or Stim V.

- Specify when to take the measurement
- Enter your specifications in the Mixed Mode window
- Stabilize voltage on the measure pin for 50 µs after the measure state
- Use the Display Analog Measure window to monitor the test

1. Select Component from the Edit/Digital menu.
2. Select the desired vector test from the Component Select window.
3. When the Step Worksheet appears, click the double arrow on the left side of Test Properties to expand the page.

   A window similar to the following appears.



4 Click the pin name, for example, 2y4, to bring up the Pin Record menu and select Meas V.

5 Click outside the menu.

A query window notes that pin types have changed and asks if you want to modify the vector.

6 Select Execute from the Query Window.

The pop-up menus will disappear, and the vector state, xxuu in this example, will all change to a (for analog).

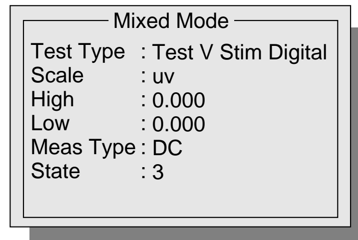
Pins	
n1g	LLLL
1a1	LLLH
2y4	aaaa
2y3	xxuu
2y2	xxuu
2y1	xxuu
1y4	xxuu

7 To indicate where in the vector you want to take the measurement, place the cursor on the desired cell and click the leftmost button.

The letter a will be replaced by M for measure.

8 Click the right mouse button to bring up the Mixed Mode window.

The following window appears.



You cannot change the Test Type or State, but you may specify Scale and Meas Type, and values for High and Low.

9 Click the Scale field to select uv, mv, or V.

10 Enter values in the High and Low fields.

11 Click the Meas Type field to select DC, Peak, RMS, or Pk-Pk.

12 Make the Measure state stable for 50 µs.

The voltage on the measure pin has to be stable for 50 µs after the measure state because of the analog instrument conversion time. To make it stable either

Don’t make any stimulus changes to the vector for 50 µs, or

change the Clock Divisor in Test_Config to 200 to allow the analog measure to be completed within the specified vector state.

13 For more information about the test set up and to monitor the test as it runs, select Tools/Display Analog Meas.

The following window appears. You can drag the window to the bottom of the screen to monitor the results as the test runs.

Pin	Node	Burst	State	High	Meas	Low	Scale	Status
3	210	65	1	5.000	0.000	4.000	V	Pass

14 To remove the Display Analog Meas window, select Close Analog Meas from the Tools menu.

Stim V Mixed Mode Vector Test

To change vector Test Properties so you can add a Stim V mixed mode vector test to your program

1 Perform steps 1–3 of the Meas V mixed mode vector test.

2 Click the pin name to bring up the Pin Record menu.

3 Click the Pin Type field and select Stim V.

4 Click outside the menu.

A query window notes that pin types have changed and asks if you want to modify the vector.

5 Select *Yes* from the Query Window.

The pop-up menus will disappear, and the vector state, xxuu in this example, will change to all a's.

6 To specify the voltage you want to stim, click the pin name again.

The Pin Record menu appears.

7 Click the Edit Analog Stim field at the bottom of the menu.

The Mixed Mode window appears.

Mixed Mode

Test Type	: Test V Stim Digital
Stim Value	: 0.000
Scale	: mv
Stim Type	: DC
Resistor	: 0 O
Wait (ms)	: 0

You cannot change the Test Type.

8 Select the Stim Value field and enter a value.

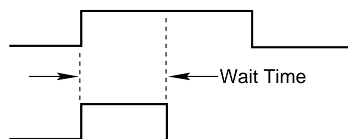
9 Click the Scale field to select a value from the pop-up window: mv or V.

10 Click the Stim Type field to select a value from the pop-up window: DC, AC 1, AC 2, or AC 3.

11 Click the Resistor field to select a value from the pop-up window: 0 ohms, 10 ohms, 100 ohms, 1 K, 10 K, 100 K, 1 M or 10 M.

12 Click Wait to specify the wait time.

The wait time specifies the delay of the vector burst after the application of the analog stim.



You may want to add time to the vector burst so that the digital state persists long enough for a proper analog sample to be taken.

5 DIODES AND ZENERS

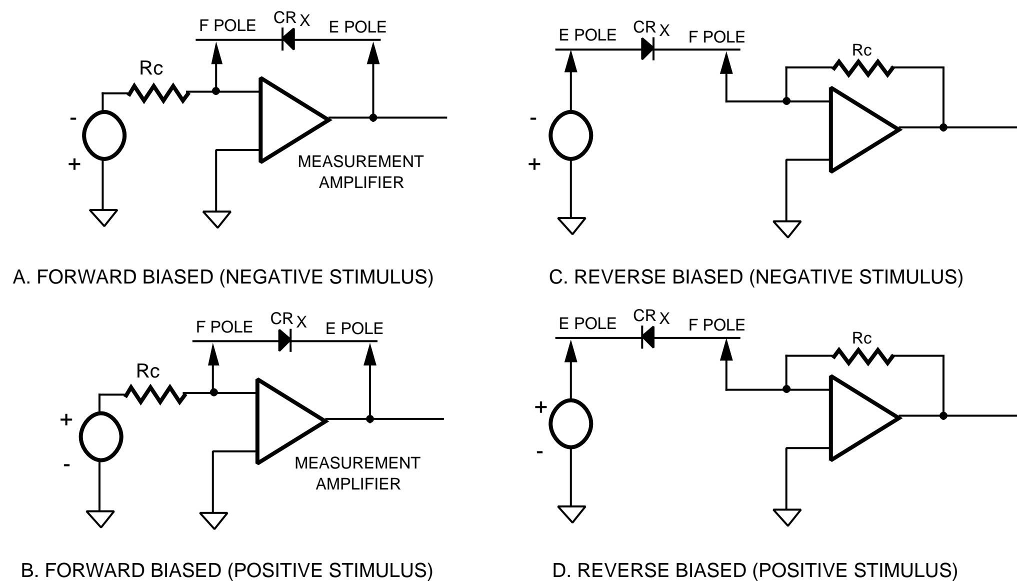
The tester performs standard diode tests in two parts:

- The forward-biased voltage drop test
- The reverse-biased current leakage test

The forward-biased drop test employs Test V Stim I mode. The reverse-biased test uses Test I Stim V mode.

In Test V Stim I, the reference resistor is in the amplifier input leg and the DUT is in the feedback loop. The voltage stimulus source and reference resistor set the stimulus current. The ATB measures the resulting voltage across the DUT.

The following figure illustrates the analog measurement configuration for typical forward and reverse-biased diode measurements.



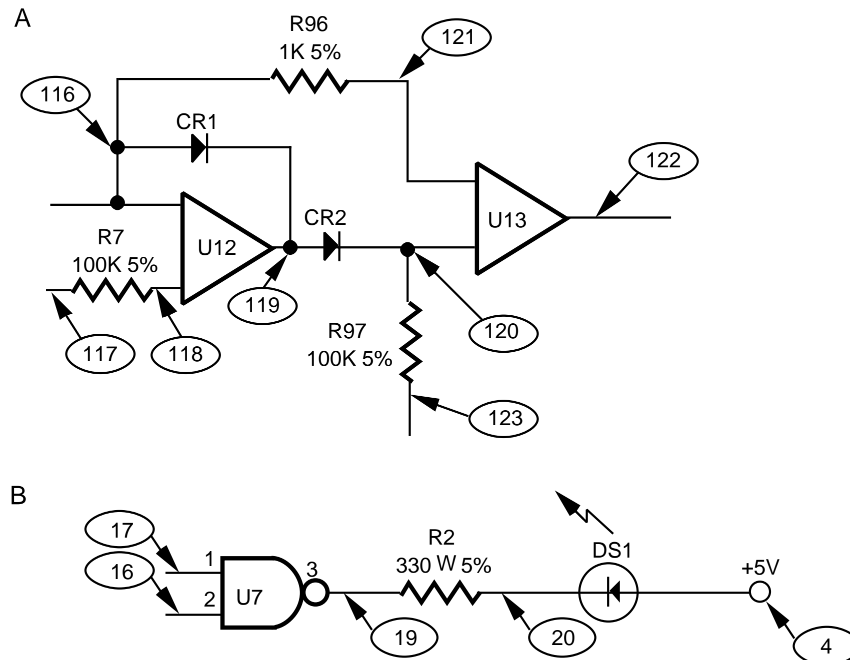
The tester applies a current stimulus for forward-bias measurements, with the diode in the feedback loop of the measurement amplifier, and measures the voltage drop of the forward biased diode junction. Reverse-bias measurements place the diode between the stimulus input and the input to the measurement amplifier, apply a voltage stimulus, and measure the reverse leakage current through the diode junction.

The analog measuring circuits measure forward bias first. If the test passes, the circuits are configured for reverse-bias measurements.

Diodes, zener diodes, and LEDs are similar in that they have a single semiconductor junction and are tested in the same manner. Voltage and current characteristics are examined to verify that the devices operate properly, even though component values may not always be well defined.

LEDs are usually examined for forward-bias characteristics only. Zeners are tested for the forward voltage drop and for the voltage at which the zener action takes place.

The following figure illustrates typical diode and LED circuits. (Sample nodes are circled.)



Testing Diodes & Zeners

When developing a diode test, determine if the diode is silicon or germanium. The type determines the shorthand test values and longhand test parameters. The default diode test assumes that the DUT is a silicon diode. More critical measurement of the forward and reverse-biased characteristics is possible by determining the actual measurement parameters from the component's data sheet.

If a diode is in parallel with a resistor, it may not be possible to perform a reverse-biased measurement . The shorthand diode test works well with normal silicon and germanium diodes, but not with other single junction semiconductor devices such as LEDs and zeners diodes. Figure B in the previous drawing is a simplified schematic representation of a typical LED circuit. The DIALCO 521-9203 LED has the parameters:

- Forward Voltage: 2.0V typical, 1.8 min. 2.8 maximum
- Forward Current: 10 mA nominal
- Reverse Voltage: 3.0 Volts maximum
- Reverse Current: 1.0µA typical, 10µA maximum

Your test program would configure the analog test circuits for Test V Stim I and set the tolerance at ±20% of expected value. Although ±20% is a relatively wide tolerance, the forward voltage drop of the LED does not require a more critical one. The diode value for the forward-biased test is the typical forward voltage parameter.

Do not connect the E pole to a power bus. Instead, connect the E pole to the cathode side of the LED and apply a negative stimulus to satisfy the polarity requirements for forward-biasing the LED. It is not necessary to perform a reverse-biased measurement of the LED, although you can do so by applying a positive stimulus and changing to Test I Stim V configuration.

Zener Test Properties configures the analog measuring circuits in Test V Stim I mode. Zener is a two-part test. The first part is a normal forward voltage drop test; the second part is a reverse zener voltage test. For voltage protection, the program will abort if the first test fails. The maximum voltage you may apply to a board if the zener is missing is 2 Volts during the forward test. Testing the forward voltage determines the presence of the device. If the zener voltage test is performed with no device, the board is exposed to at least 13 Volts. The default current stimulus value for this test is 10 mA.

Zener Diodes in parallel with Capacitors

When you test zener diodes that are in parallel with capacitors, it is important to have a discharge test page after the zener test to discharge any potential charge held by the capacitor.

Programs generated under F.0 automatically add a discharge page to zener tests. In programs generated before F.0, you should manually add the discharge test page to protect your test system from the potential damage that could occur as a result of high guard currents from following test steps.

Range and Accuracy

The Range column states the testable range of diode and zener values. The accuracy of a test technique at a given range is opposite each row of ranges. (Device tolerance also influences accuracy.) The Stimulus column displays the shorthand stimulus applied within the stated range.

Test	Range	Accuracy	Stimulus
Forward Voltage	0.00 to 9.99 V	0.02 % ± 1 mV	10 mA
Zener Voltage	0.00 to 9.99 V*	0.02 % ± 10 mV	10 mA
Reverse Leakage	0 to 999 µA	5 %	3.000 V DC

*99.99 V with the High Voltage Option

The following factors influence shorthand test accuracy:

- Shorthand accuracy tolerance
- Guard ratio error tolerance

Step Worksheet Editing

You can edit a diode or zener test step at any time from the Step Worksheet. A Step Worksheet contains a menu bar, Component Properties, and Test Properties.

To access a diode or zener Step Worksheet from the Main menu, select

1. The board program
2. Edit
3. Semi
4. Diodes or Zeners
5. A diode ID (CR1, for example), or zener ID (VR1, for example) from the Component Select window.

Component Properties Editing

Refer to the **Z1800-Series Programmer's Guidebook**, Chapter 3, for specific details about editing the Component Properties.

Note that diodes do not have value or tolerance fields because the forward voltage test values are predetermined by the software and reported in Test Properties High and Low fields. Zeners have a single tolerance percentage field.

Test Properties Editing

Diode and zener Test Properties contain the parameters to execute the test step. To edit Test Properties, select Edit from the menu bar, then Test Properties—or simply place the cursor on the data field you wish to edit.

An example of a diode Step Worksheet with pop-up menus appears below.

Beta
Cap Phase
CapScan
Capacitor
DigFuncProc
Diode
Discharge
External Program
IEEE
Inductor
No test
Resistor
Test I Stim V
Test I Stim V Stim V
Test V
Test V Stim I
Test V Stim I Stim V
Test V Stim V
Test V Stim V Stim V
Transistor
Zener

18xx Windows mode-init_com
Edit Options Tools Save Revert Validate Quit
Component Properties [↑]–[↓]
+ID:CR1 Name: N914 Desc:
Device Type: **Diode**
Number of Pins:2
Test Properties [↑]–[↓]
Options
Pre Post Cntrl
Indicators
Current Page
Page 1 of 1
Test Type: **Diode**
Test Data
Scale: mv Reverse Test : **Yes**
High: 840 Reverse Curr (ua): 10
Low: 560 Stim Node On : **Cathode**
Forward Curr (ma) : 10,000
Stimulus : Pin 1 (4)
Measure : Pin 2 (84)
Guard :
Wait (ms) : 0
Squelch (ms): 0
Controls
Wire Mode: 3 Precise: Off Averaging: 10
Guard Mode: Active
C:\TPD\DEMO-ICT START CANCEL SOF HLD RPT CRT

uv Default
mv 6 decimal
V

Yes
No

Cathode
Anode

APC
Analog template
Beta-NPN
Beta-NPN
CapScan
Capacitor
DigFuncProc
Diode
Discharge
Inductor
Potentiometer
Resistor
Rheostst
Rpack-DB
Rpack-DI
Rpack-DT
Rpack-SB
Rpack-SI
Rpack-ST
Transistor-NPN
Transistor-PnP
Zener

Test Properties fields specific to diodes are described in the following table.

Upper Test Properties Area	
Field	**Description**
Test Type:	The type of test configuration used in current Test Properties. Recommended for diodes:
Diode	Shorthand diode test
IEEE	IEEE instrument test
Test I Stim V	Voltage stimulus and current measurement test (for reverse leakage)
Test V Stim I	Current stimulus and voltage measurement test (for forward or breakdown—zener—voltage)
Test Data/Middle Test Properties Area	
Scale	Value field’s unit modifier based on Test Type
Diode	uv, mv, V
Test I Stim V	na, ua, ma
Test V Stim I	uv, mv, V
High	High limit of forward voltage drop test. Higher measurement sets fail flag.
Low	Low limit of forward voltage drop test. Higher measurement sets fail flag
Reverse Test	YES or NO. When YES, performs reverse leakage test.
Reverse Curr (ma)	When Reverse Test is YES, enter number in range of 0 to 999 (ua).
Stim Node On	Anode or Cathode, to control polarity of stimulus voltage and orientation of diode in test circuit.

An example of a zener Step Worksheet with pop-up menus appears below.

Beta
Cap Phase
CapScan
Capacitor
DigFuncProc
Diode
Discharge
External Program
IEEE
Inductor
No test
Resistor
Test I Stim V
Test I Stim V Stim V
Test V
Test V Stim I
Test V Stim I Stim V
Test V Stim V
Test V Stim V Stim V
Transistor
Zener

18xx Windows mode-init_com
Edit Options Tools Save Revert Validate Quit
Component Properties [↑]–[↓]
+ID: VR2 Name: 18v zener Desc:
Value: 18 volts Device Type: **Zener**
Tol: 5 Number of Pins:2
Test Properties [↑]–[↓]
Options: Pre Post Cntr
Indicators
Current Page: Page 1 of 1
Test Type:**Zener**
Test Data
Value: 18
Scale: V
High : 18.9
Low : 17.1
Forward Test : **Yes**
Forward Volt (mv) 900
Stim Node On : **Anode**
Reverse Curr (ma) : 10
Stimulus : Pin 1 (38)
Measure : Pin 2 (10)
Guard :
Wait (ms) : 0
Squelch (ms) 0
Controls
Wire Mode: 3 Precise: Off Averaging: 10
Guard Mode: Active
C:\TPD\DEMO-ICT START CANCEL SOF HLD RPT CRT

uv Default
mv 6 decimal
V

Yes
No

Cathode
Anode

APC
Analog template
Beta-NPN
Beta-NPN
CapScan
Capacitor
DigFuncProc
Diode
Discharge
Inductor
Potentiometer
Resistor
Rheostst
Rpack-DB
Rpack-DI
Rpack-DT
Rpack-SB
Rpack-SI
Rpack-ST
Transistor-NPN
Transistor-PnP
Zener

Test Properties fields specific to zeners are described in the following table.

Upper Test Properties Area	
Field	**Description**
Test Type:	The type of test configuration used in current Test Properties. Recommended for zeners:
Zener	Shorthand diode test
Test I Stim V	Voltage stimulus and current measurement test
Test V Stim I	Current stimulus and voltage measurement test
Test Data/Middle Test Properties Area	
Zener	uv, mv, V
Test V Stim I	uv, mv, V
Test I Stim V	na, ua, ma
Test V Stim I	uv, mv, V
High	High limit of forward voltage drop test. Higher measurement sets fail flag.
Low	Low limit of forward voltage drop test. Higher measurement sets fail flag
Forward Test	YES or NO. When YES, performs forward voltage test.
Forward Volt (mv)	When Forward Test is YES, enter number in range of 0.001–1200 (mv).
Stim Node On	Anode or Cathode, to control polarity of stimulus voltage and orientation of diode in test circuit.
Reverse Curr (ma)	Range = 0 to 250 (ma)

The Test Type field allows you to select an analog subsystem test configuration. Test types can either be shorthand or longhand. The shorthand test type for diodes is Diode, and for zeners, Zener.

You can select any of the test types available in the Test Type pop-up menu. However, the standard test types for diodes and zeners are shown above.

Refer to the **Z1800-Series Programmer's Guidebook**, Chapter 5, for a discussion of longhand test and test types.

The Value field (zeners only) represents the zener's rated voltage. This portion of the zener Step Worksheet applies a selectable current to the zener diode in the reverse (zener) direction.

The Forward Test field, when Yes, represents the forward voltage test, placing the zener in a forward-biased configuration using a constant current. The zener test is patterned after the diode test, but focuses on the zener (reverse breakdown) voltage rather than forward voltage.

The Forward Volt (mv) field, when Forward Test is Yes, represents the nominal forward voltage drop limitation. Most zeners have nominal forward voltage drops in the range of 700 to 800 mv, although it is occasionally necessary to program larger or smaller voltages due to variations in specifications. The range for this field is 0.001 to 1200 mv.

For diodes only, the Reverse Test field applies to standard diodes. When Yes, this field instructs the tester to measure a diode's reverse current leakage characteristic by applying a voltage of 3.0 VDC (reverse bias) to the diode and then measuring the amount of current passing through. Enter a value in the range of 0–999 (na), which will be the maximum acceptable leakage current through the diode in the Reverse Curr field. A measured value greater than that will result in a test failure. If you set Reverse Test to No, no reverse leakage test is performed.

IMPORTANT
The current should not exceed the maximum rated zener current.

For zener tests, the Reverse Curr (ma) field represents the stimulus current used to measure the zener voltage. The current programmed is related to the wattage and voltage of the zener. The default is 20 ma.

The Stim Node On field allows you to select the polarity of the zener with respect to the Stim and Meas terminals. Select either Anode or Cathode. With this field, you can control the orientation of the diode or zener in the test circuit and the configuration of the analog test subsystem.

The Squelch time on the Zener worksheet is applied both at the beginning of the page and end of the page. At the end of the Zener page, the stimulus is turned off and waits for the amount of time you entered in the Wait and Squelch fields in order to discharge the nodes associated with your Zener test.

6 Discharge

The purpose of Discharge is to discharge capacitors on the board under test before running a test. Discharge test steps run at the beginning of a program, and are listed in the Intc section.

Discharge Testing

Discharge Test Properties discharge only those nodes that have been programmed for discharge. Residual charges can remain on nodes in the circuit that have not been programmed for discharge. This situation can happen if there are storage elements such as capacitors or batteries that are isolated from the discharge node by an impedance. Although the passing voltages may reappear due to the memory effect of the large cap.

In addition, you can create an APC test step in the discharge section to test a range of nodes for contact with the board under test early in the program. This Global APC feature is particularly useful if your boards are dirty or the fixture is unreliable to see if test execution should be aborted and the board under test recontacted.

Refer to page 3 for more information about adding an APC test step.

Discharging is essential to prevent damage to the board and to the tester relays. You can also insert a discharge routine as Test Properties in a capacitor Step Worksheet when required to discharge a capacitor.

To edit a discharge routine from the Main menu, select:

1. Edit
2. Intc
3. Discharge
4. A discharge ID from the Component Select window

Editing

Refer to the **Z1800-Series Programmer's Guidebook**, Chapter 3, for general information about editing Component Properties. Discharge Step Worksheets, however, have no value or tolerance fields.

Test Properties Editing

To edit Discharge Test Properties, select Edit from the menu bar, then Test Properties—or simply place the cursor on the data field you wish to edit.

An example of a discharge Step Worksheet with pop-up menus appears below.

Beta	Resistor
Cap Phase	Test I Stim V
CapScan	Test I Stim V Stim V
Capacitor	Test V
DigFuncProc	Test V Stim I
Diode	Test V Stim I Stim V
Discharge	Test V Stim V
External Program	Test V Stim V Stim V
IEEE	Transistor
Inductor	Zener
No test	

18xx Windows mode-init_com

Edit Options Tools Save Revert Validate Quit

Component Properties [↑]–[↓]

+ID: C8 Name: 18v zener Desc:

Value: 18 volts
Tol: 5

Device Type: **Discharge**
Number of Pins:2

Test Properties [↑]–[↓]

Options: Pre Post Cntrl

Indicators

Current Page: Page 1 of 1

Test Type:**Discharge**

Test Data

Threshold : 5
Scale : mv

Timeout (ms): 25000

Measure : Pin 1 (46)
Guard : Pin 2 (32)

Controls

Wire Mode: 3
Guard Mode: Active

Precise: Off

Averaging: 10

C:\TPD\DEMO-ICT START CANCEL SOF HLD RPT CRT

uv	Default
mv	6 decimal
V	

APC	Resistor
Analog template	Rheostst
Beta-NPN	Rpack-DB
Beta-NPN	Rpack-DI
CapScan	Rpack-DT
Capacitor	Rpack-SB
DigFuncProc	Rpack-SI
Diode	Rpack-ST
Discharge	Transistor-NPN
Inductor	Transistor-PnP
Potentiometer	Zener

Upper Test Properties Area

Field	Description
Test Type:	The type of test configuration used in current Test Properties.
Discharge	Shorthand discharge test.
Test Data/Middle	**Test Properties Area**
Threshold	Maximum residual voltage of Scale for proper discharging. Range = 0–999.
Scale	Threshold field’s unit modifier. Choices are mv, V
Timeout	Maximum time allowed to reach discharge voltage level. Range = 0–32000.

Discharge steps are not automatically added when capacitors are added by hand. Capacitors above 50 uF must have an associated Discharge step.

The Test Type field allows you to select an analog test configuration or type the tester will use to execute the step. The test type for discharge steps is Discharge.

The Threshold and Scale fields define the voltage the capacitor will be discharged to. The default is set to 5 mV. Thresholds should not be set too high, otherwise tester relays can be damaged, depending on the size of the capacitor and its residual charge.

The Timeout field represents the maximum time allowed for the discharge test to reach its acceptable discharge voltage level. If the capacitor is not discharged within this amount of time, the discharge test will fail. Enter a value in the range of 0 to 32,000 ms. If discharge is achieved before the time expires, the test will automatically terminate.

Adding Discharge Test Step for Global APC

Dirty boards with an excess of flux residue or an unreliable fixture can cause contact problems between the tester and the DUT. In such cases it is advisable to test for board contact problems early in the test program. The Global APC function provides this test capability.

Global APC should be done in the Discharge section after all the discharge steps have executed correctly. Using Global APC to test for board contact will weld reed relays when executed while there are charged up capacitors present on the board. It may be prudent to run Discharge again after the APC test because the APC test itself could charge up some capacitors. (This situation is unlikely, however, since the stimulus time is short.)

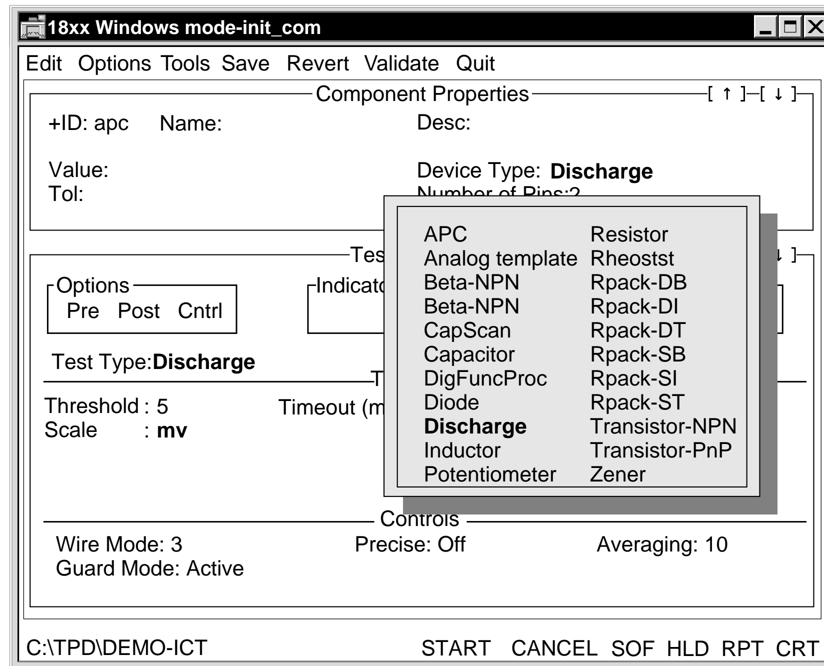
To test for uncontacted nodes, Global APC uses a three-pass approach. First, every node is measured for the specified current threshold while stimulating a -3 V stimulus. Then the failing nodes (those below the threshold) will be tested in the same way with +3 V stimulus. Still failing nodes are then tested with an AC stimulus and remaining failing nodes are reported. The last phase is optional and can be controlled by the Slow/Fast flag in Test Properties since it is considerably slower than the DC test. The AC test is meant to find nodes contacted only by small capacitors which cannot otherwise be found.

Should the APC test fail, the General Fail flag and the APC Fail flag will be set.

The generator token for APC is APC, and it follows the same syntax as Shorts—SH.

To create the Global APC Step Worksheet

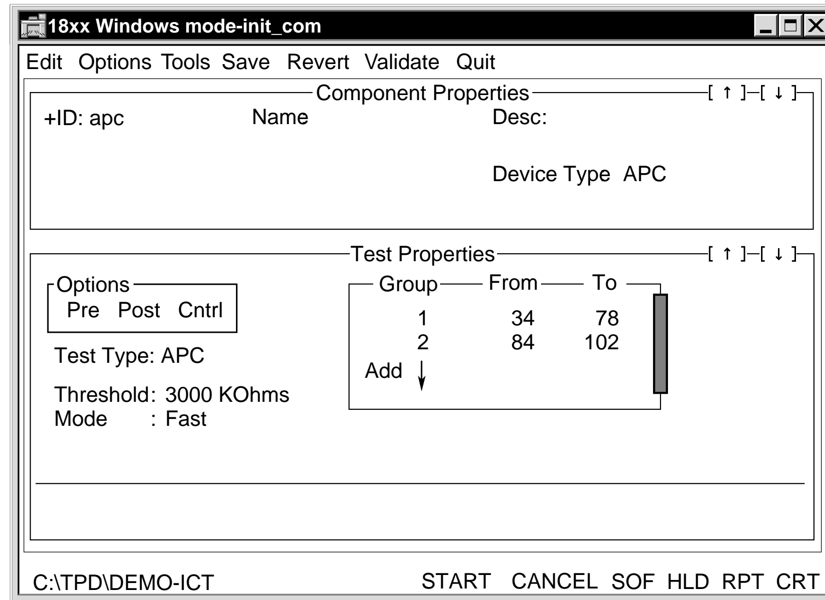
1 Add a Step Worksheet at the end of the Discharge section.
2 When Component Properties appears, type an appropriate identification such as apc in the ID field.
3 Click Device Type and select APC from the pop-up menu.



Be aware that range for the APC Threshold is 300 MOhms to 12KOhms.

1 Select Tools/Generate Test.
2 When the Test Properties page appears, fill in the node range you want to test APC on. The syntax is the same as it is in a shorts test.

Be sure to exclude from the APC node range those nodes (such as batteries) that cannot be discharged. All the nodes listed will be connected together internally, and charged up nodes would weld together. Use the Short Test node range as a starting point, and exclude further nodes that are untestable with APC.



The Test Type field in Test Properties is locked and cannot be modified.

3 Click the Mode field. A pop-up window appears allowing you to specify Fast or Slow. Use Fast for a ±DC test. Use Slow for ±DC and AC1 tests.

7 INDUCTORS

The standard inductor is tested in Test I Stim V mode.

Inductors that are too small or too large to be measured accurately for inductance can be tested for presence on the board by measuring DC resistance. Most inductors have low DC resistance and need to be declared as Ignore groups in the Intc test section.

The PRISM-Z (PRecision Integrated Signal Measurement) module is available as an option and can be used for Inductor tests. Refer to the **Z1800-Series PRISM-Z User's Guide** for a complete discussion about the PRISM-Z test types available for Inductor tests.

Range and Accuracy

Use the following listing as a guide for range and accuracy

Range	Accuracy		
	3-Wire	6-Wire	Stimulus*
10 to 29.99 μH		10 % ±10 μH	0.3V pk to pk AC3
30.0 to 299.9 μH		10 % ±10 μH	0.3V pk to pk AC3
300 to 2999 μH		5 % ±10 μH	0.3V pk to pk AC3
3.00 to 29.99 mH	8 % ±10 μH	5 % ±10 μH	0.3V pk to pk AC2
30.0 to 2999 mH	8 %	NA	0.3V pk to pk AC2
3.00 to 29.99 H	8 %	NA	0.3V pk to pk AC1

*AC1 = 159.1 Hz; AC2 = 1.591 kHz; AC3 = 15.91 kHz
System inductance: 5 μH typical
Resistive component of inductor: measured and subtracted.

Shorthand test accuracy is affected by the following factors:

- Shorthand system accuracy
- System resistance, capacitance, or inductance (if not subtracted)
- Guard ratio error tolerance
- Device-under-test (DUT) tolerance

Step Worksheet Editing

You can edit an inductor test step at any time from the Step Worksheet. The Step Worksheet contains a menu bar, Component Properties, and Test Properties.

To access an inductor Step Worksheet from the Main menu, select

1. The board program
2. Edit
3. Passive
4. Inductors
5. An inductor ID, such as L1 or L2, for example, from the Component Select window

Component Properties Editing

Refer to the **Z1800-Series Programmer's Guidebook**, Chapter 3, for a description of the fields common to analog component testing. Inductors have a single tolerance field.

Test Properties Editing

An example of an inductor Step Worksheet with pop-up menus appears below.

Beta
Cap Phase
CapScan
Capacitor
DigFuncProc
Diode
Discharge
External Program
IEEE
Inductor
No test
Resistor
Test I Stim V
Test I Stim V Stim V
Test V
Test V Stim I
Test V Stim I Stim V
Test V Stim V
Test V Stim V Stim V
Transistor
Zener

18xx Windows mode-init_com
Edit Options Tools Save Revert Validate Quit
Component Properties [↑]–[↓]
+ID: L1 Name: 1 mH Desc:
Value: 1 mh Device Type: **Inductor**
Tol: 10 Number of Pins:2
Test Properties [↑]–[↓]
Options: Pre Post Cntrl
Indicators
Current Page: Page 1 of 1
Test Type:**Inductor**
Test Data
Value: 1
Scale: mh
High : 1.1
Low : 0.9
Stimulus : Pin 2 (68)
Measure : Pin 1 (33)
Guard :
Wait (ms) : 0
Squelch (ms) : 0
Controls
Wire Mode: 3
Guard Mode: Active
Precise: Off
Higuard: Off
Averaging: 1
C:\TPD\DEMO-ICT START CANCEL SOF HLD RPT CRT

uh
mh
H
Default
6 decimal

APC
Analog template
Beta-NPN
Beta-NPN
CapScan
Capacitor
DigFuncProc
Diode
Discharge
Inductor
Potentiometer
Resistor
Rheostst
Rpack-DB
Rpack-DI
Rpack-DT
Rpack-SB
Rpack-SI
Rpack-ST
Transistor-NPN
Transistor-PnP
Zener

Test Properties fields specific to inductor test are explained in the table below.

Refer to the **Z1800-Series Programmer's Guidebook**, Chapter 3, for information about Test Properties fields common to analog component tests.

Upper Test Properties Area	
Field	**Description**
Test Type:	The type of test configuration used in current Test Properties. Recommended for inductors:
Inductor	Shorthand inductor test
Resistor	Shorthand resistor test for inductors too small or too large for inductance
Test I Stim V	Voltage stimulus and current measurement test
Test V Stim I	Current stimulus and voltage measurement test

Test Data/Middle Test Properties Area	
Value	Numeric field specifying nominal expected value of Scale. Range = 0–1000.
Scale:	Value field’s unit modifier based on Test Type
Inductor	uh, mh, H
Resistor	Ohms, Kohms, Mohms
Test I Stim V	na, ua, ma
Test V Stim I	uv, mv, V
Wait (ms)	0 to 32000 ms. Added to default wait of 3 ms typical.
Squelch (ms)	0 to 32000 ms. Repeatable initial condition to remove stored energy.

The Test Type field allows you to select an analog test configuration or type the tester will use to execute the step. Test types can be either shorthand or longhand. The shorthand test type for inductors is Inductor.

8 INTERCONNECTS

The Intc menu includes Discharge, Jumpers, Continuities, Ignores, Merge_Sc, Shorts, and Opens.

The interconnections test categories above are listed in the order of test execution. Discharge tests are not interconnections but are executed in the Intc section to ensure that all residual board charges are dissipated at the beginning of a program.

See the Discharge Test Steps section for details about global discharging.

Continuities Tests and Editing

Continuities tests verify proper connectivity between node groups. Continuities are groups of node number sets that are electrically connected in the same network. Continuities differ from jumpers. Jumpers are usually an assembled component that may be reported missing. Continuities are not physical components, but such things as multiple nodes on a board trace, or the presence of a trace, end to end.

For example, a continuity between nodes 12 and 34 comprises a continuity group. Nodes 56, 78, and 90, if electrically connected, would comprise a second group. Each group would be assigned a group number, starting with 1. The group number is reported in the event of a failure.

Each expected continuity should be entered in Test Properties. The tester measures resistance between the indicated nodes. If the measurement is equal to or less than the continuity threshold, the nodes pass the continuity test. If the measurement exceeds the threshold, the continuity fails.

Continuities are also tested in the Ignores section to prevent shorting of other nodes, which are ignored in the shorts test.

The measurement threshold is adjustable from 1 to 50 ohms. In other words, a continuity can be defined as having a resistance as high as 50 ohms. The default value for a continuity's measurement threshold is 5 ohms.

To edit a continuity Step Worksheet from the Main menu, select:

1. Edit
2. Intc
3. Continuities
4. A continuities ID from the Component Select window

Component Properties Editing

Component Properties contains fields of descriptive data about the component being tested. Test Properties, however, determines how the test executes.

Refer to the **Z1800-Series Programmer's Guidebook**, Chapter 3, for a description of all fields other than Value and Number of Conts.

An example of a Continuities Component Properties appears below.

The Device Type field is read-only for continuities tests.

Test Properties Editing

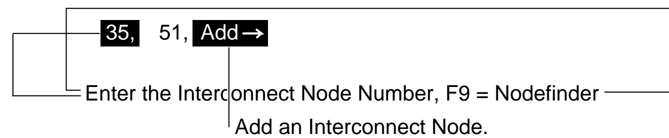
Continuities Test Properties contain the parameters to execute the test step. To edit Test Properties, select Edit from the menu bar, then Test Properties—or simply place the cursor on the data field you wish to edit.

An example of a continuities Step Worksheet appears below.

To edit a group of nodes:

1 Select a group field.

A node editor window appears

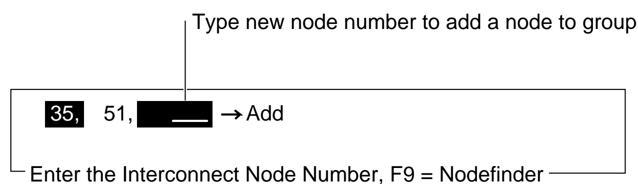


2 To edit a node, place the cursor on the node you want to edit and type the new node number.

The Enter key advances the cursor to the next field.

3 To add nodes, select the Add field by a single mouse click or by pressing Enter.

Type a node number in the empty field.



4 Select Save to save changes.

Select Revert to remove edits since last saved setup.

Test Properties fields

The following is a description of the Continuities Test Properties fields:

Field	Description
Options	Pre-Test, Post-Test, and Controls. Read-only.
Test Type: Continuity	The type of test configuration used in current Test Properties. Continuities test. Read-only field.
Threshold	Threshold value in Ohms. Range = 1 – 50. Default = 5.
Group	Number of a node group.
Nodes	Nodal address(es) of node(s) in a group.

The Test Type field is always Continuity for continuities tests.

The Threshold field represents the measurement threshold value in ohms.

The Group field begins with 1. The Nodes fields associated with a group are shown immediately to the right of the group number. Only the nodes listed are associated with each group. Use numbers only to identify nodes.

Ignores Testing

Ignores testing is a method of registering low impedance or unpredictable paths to prevent false reporting as a short during Shorts testing. Very low resistance inductors, very large capacitors, potentiometers, and switches should also be entered into the Ignores table to prevent shorts failures.

Ignores verifies that no shorts exist between any nodes in an Ignores group and any other point on the printed circuit board not in the group. An Ignores group passes if the resistance between any node in the group and all other nodes exceeds the ignore threshold. The Threshold field represents the measurement threshold value in Ohms. An Ignores group fails and reports as a short if any Ignores group node has less resistance to a node outside the group.

The threshold is adjustable from 2 to 50 ohms. The default value is 5 ohms.

The Threshold field is the threshold for the comparison to outside nodes. Any outside node having less resistance than Threshold will fail as a short.

Nodes listed in an ignores group are not tested against each other but rather against nodes outside the group, including other Ignores groups. If a short exists on an external node it will be reported.

To edit an Ignores Step Worksheet from the Main menu, select:

1. Edit
2. Intc
3. Ignores
4. An ignores ID from the Component Select window

Ignores and continuities have the same editing features. Refer to the Continuities section for details about editing the Step Worksheet.

Jumpers Testing

Jumpers are physical wires on the board under test that can be diagnosed erroneously as missing components if not accounted for in the Jumpers section. Jumpers may be connections of signal traces on the board under test, such as jumper blocks, zero-ohm resistors, and cuttable board traces. The difference between a jumper and a continuity is that a jumper is an identifiable component with a name.

A jumper is tested as a set of electrically connected nodes, isolated from all other nodes. Each jumper group is given a group number as is the case with continuities and other interconnection tests (except Discharge).

The measurement threshold is adjustable from 1 to 50 ohms. In other words, a jumper can be defined as having a resistance as high as 50 ohms. The default value for a jumper's measurement threshold is 5 ohms. If the jumper you are testing has a value below 5 ohms, you must enter that value.

The Threshold field represents the measurement threshold value in Ohms.

To edit a jumper Step Worksheet from the Main menu, select

1. Edit
2. Intc
3. Jumpers
4. A jumper ID from the Component Select window

Jumpers and continuities have the same editing features. Refer to the Continuities section for details about editing the Step Worksheet.

Merge_SC (Merge Special Case) Testing

The Merge_SC step provides two functions.

First, it is a summary table of all nodes that will not be reported as shorts in the standard Shorts test. This table is composed of all continuity groups, jumpered nodes, and those nodes specified as ignores. Programmers should examine this table to verify that all nodes and node groups listed, in fact, should not be tested in the regular Shorts test.

Second, Merge_SC tests nodes itself. All continuity groups, jumpered, and ignored nodes are tested for shorts against all other nodes outside their own group. This includes both nodes in other MERGE_SC groups as well as all others that fall into the ranges listed in the following SHORTS Step Worksheet test steps.

During program debug, the Merge_SC section must be run prior to the Shorts step, otherwise the shorts testing algorithm will see all of the Merge_SC nodes as shorts.

Shorts Tests and Editing

A shorts group is a set of node numbers tested to verify that each node is electrically isolated from all the others in the group. (The Merge_Sc—merge special cases—Step Worksheet summarizes all exceptions to the shorts node range.) You can define multiple shorts groups. The nodes in each group will be checked against all other node groups.

Usually the ranges of nodes cover the lowest numbered node to the highest numbered node in the fixture.

The Threshold field represents the measurement threshold value in ohms.

The Wait field allows you to enter a wait time (in ms) for short measurements. You can use this feature to prevent large capacitors from being reported as shorts. The wait time you enter is applied when a measurement indicates a short. A secondary measure is taken, and if a short is still indicated, the short is reported; if the delayed measure passes, then the short is not reported.

The wait time you enter on the Shorts Test Properties applies to the Short test and Merged_SC testing.

Shorts Specifications:

Range: 0.0 to 100.00 Ohms
Resolution: 0.1 Ω
Accuracy: 5% ±0.5 Ω
Stimulus: 0.2 V dc
Default: 5 Ohms

To edit a shorts Step Worksheet from the Main menu, select

1. Edit
2. Intc
3. Shorts
4. A shorts ID from the Component Select window

Shorts and continuities have the same editing features. Refer to the Continuities section for details about editing the Step Worksheet.

Opens Testing

Opens tests are used only for the fixture selftest and should not be part of an in-circuit test program. Used for fixture verification, this test measures probe resistance. As the inverse of the shorts test, it reports all the nodes not in contact with the shorting plate. You will need a shorting plate for an opens test.

To edit an opens Step Worksheet from the Main menu, select

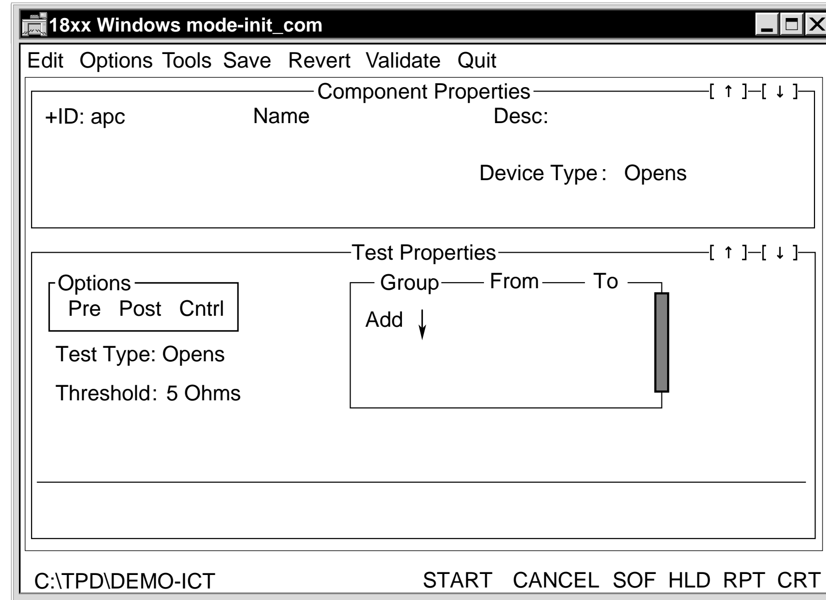
1 Edit

2 Intc

3 Opens

4 An opens ID from the Component Select window

A window similar to the following appears



The opens range should include the range of nodes that pertain to the specific fixture.

Nodes showing a higher resistance value than the program threshold are reported as failing nodes. You must replace such nodes before testing can begin.

9 LINEAR ANALOG

Linear tests can be tests of special analog devices requiring power, or they can be tests for measuring voltage at some point at a nodal address. Devices in the Linear category can include operation amplifiers, voltage regulators, comparators, and even relays. (To test special analog devices with power off, use the PwrOff category.)

Shorthand test accuracy is affected by the following factors:

- Shorthand system accuracy
- System resistance, capacitance, or inductance (if not subtracted)
- Guard ratio error tolerance
- Device-under-test (DUT) tolerance

Longhand test accuracy is affected by the following factors:

- Stimulus tolerance
- Measurement tolerance
- Guard ratio error tolerance
- Device-under-test (DUT) tolerance.

You can edit a linear test step at any time from the Step Worksheet. The Step Worksheet contains a menu bar, Component Properties, and Test Properties, all of which appear below.

To open an analog linear Step Worksheet from the Main menu, select

1. Edit
2. Linear
3. A linear ID from the Component Select window

Editing

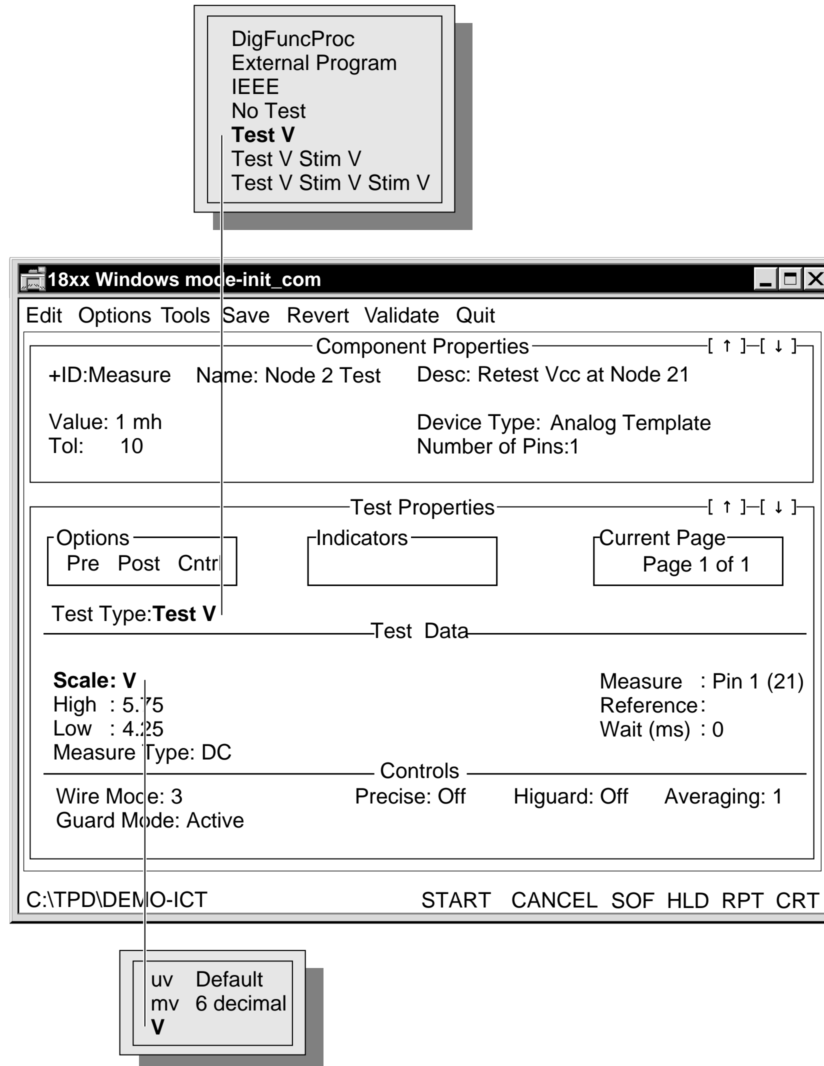
Component Properties contains fields of descriptive data about the component being tested.

Refer to the **Z1800-Series Programmer's Guidebook**, Chapter 3, for a description of the fields common to component testing.

Linear tests, however, have a single Device Type field, Analog Template.

Test Properties Editing

Linear Test Properties contain the parameters to execute the test step. To edit Test Properties, select Edit from the menu bar, then Test Properties—or simply place the cursor on the data field you wish to edit. An example of a linear Step Worksheet with pop-up menus appears below.



Test Properties fields specific to linear test are explained in the table below.

Refer to the **Z1800-Series Programmer's Guidebook**, Chapter 3, for information about Test Properties fields common to analog component tests.

Upper Test Properties Area

Field	Description
Test Type:	Test configuration for the current Step Worksheet. For Linear:
External Program	Accesses an external program.
IEEE	Test using IEEE-488 bus peripheral equipment.
Test V	Longhand voltage test.
Test V Stim V	Longhand voltage stimulation and voltage measurement
Test V Stim V, Stim V	Dual stimulus

Test Data/Middle Test Properties Area

Test V :

Scale	Measurement-related modifier—uv, mv, V—of High and Low values.
High	Upper limit for a passing measurement. Range = -1000.00000 to1000.000000
Low	Lower limit for a passing measurement. Range = -1000.00000 to1000.000000
Measure Type	DC, Peak, RMS, or Pk-Pk (peak to peak)
Measure	Pin/node number(s) at which measurement is taken. 5 nodes maximum. Range = 0–2047.
Reference	Pin/node number(s) of the ground reference point(s). 10 nodes maximum.
Wait (ms)	0 to 65534 ms. Added to default wait of 3 ms typical.

Test V Stim V:

Scale, High, & Low	Stimulus-related fields. (See Test V above.)
Measure Type	DC, Peak, RMS, or Pk-Pk (peak to peak)
Stim Value	Value of stimulus. Range = -1000.00000 to 1000.000000
Scale	Stimulus-related modifier— mv, V—of High and Low values.
Stim Type	DC, AC1, AC2, AC3
Resistor	Current-limiting resistor value. Select from: 0 ohms, 10 Ohms, 100 ohms, 1 KO, 10 KO, or 100 KO, 1 megohm, 10 megohms.
Stimulus	Pin/node number(s) to which stimulus applied. 5 nodes max.
Measure	Pin/node number(s) at which measurement is taken. 5 nodes max.
Reference	Pin/node number(s) of the guard point(s). 10 nodes max.
Wait (ms)	0 to 65534 ms. Added to default wait of 3 ms typical.
Squelch (ms)	0 to 65534 ms. Repeatable initial condition to remove stored energy.

Test V Stim V Stim V:

Scale, High, & Low	Measurement-related fields. (See Test V above.)
Measure Type	DC, Peak, RMS, or Pk-Pk (peak to peak)
Stim 1 Value	Value of stimulus. Range = -1000.0 to +1000.0
Stim 1 Scale	mv or V
Stim 1 Type	DC, AC1, AC2, AC3
Resistor 1	Current-limiting resistor value. Select from: 0 ohms, 10 ohms, 100 ohms, 1 KO, 10 KO, or 100 KO, 1 megohms, 10 megohms
Stim 2 Value (V)	-6.4 to +6.4 V
Resistor 2	10 ohms, 100 ohms, 1 KO
Stimulus 1	Same as Test V Stim V. Note: Stim 1 and Stim 2 nodes can't be in same group of 16 nodes.
Stimulus 2	Same as Test V Stim V. Note: Stim 1 and Stim 2 nodes can't be in same group of 16 nodes.
Measure	Pin/node number(s) at which measurement is taken. 5 nodes max.
Reference	Pin/node number(s) of the guard point(s). 10 nodes max.
Wait (ms)	0 to 65534 ms. Added to default wait of 3 ms typical.
Squelch (ms)	0 to 65534 ms. Repeatable initial condition to remove stored energy.

External Program:

Scale	pico, nano, micro, milli, unit, Kilo, Mega
High, Low	Upper and lower limits of passing measurements.
Mem Req	Swap space needed for external program to run.
E pole	Pin/node number(s) to which stimulus applied. 5 nodes max.
F pole	Pin/node number(s) at which measurement is taken. 5 nodes max.
G pole	Pin/node number(s) of the guard point(s). 10 nodes max.
IEEE	See the IEEE section of the Z1800-Series Options Manual for details.

The Linear Test Type allows you to select a test configuration or test type to execute the test step. Linear test types are either longhand or IEEE.

You can select any of the test types available in the Test Type pop-up at left. If the device test does not already exist, Test Properties initially comes up as Test Type, No Test.

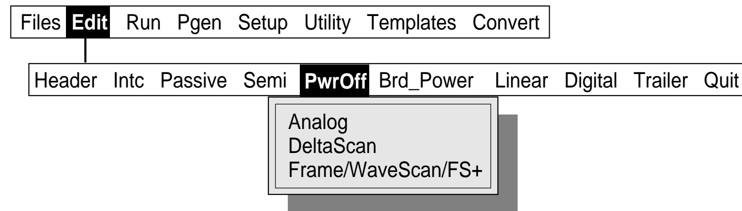
10 Power-Off Longhand Analog

The PwrOff test category accommodates special analog devices that do not require power to test, such as thermistors, MOV devices, varistors, thyristors devices requiring explicit control of all voltages and current, and tests employing IEEE instrumentation. The PwrOff category also provides access to the MultiScan tests: FrameScan, WaveScan, and DeltaScan.

See the **Multiscan User's Guide** for additional information about the PwrOff category.

To access either Analog or MultiScan test sections from the Main menu, select:

1. The board program
2. Edit
3. PwrOff
4. Analog, DeltaScan, or Frame/WaveScan/FS+

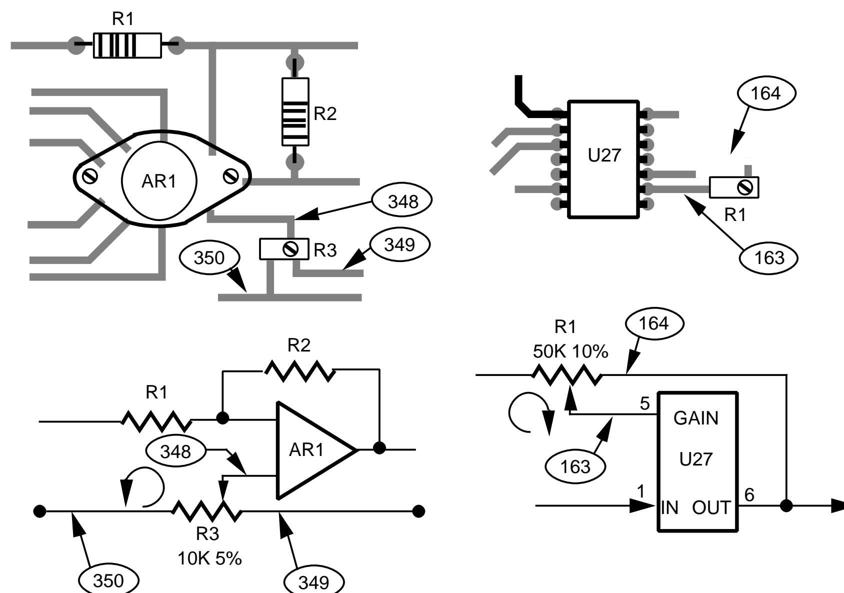


Use the Linear category to perform power-on analog longhand testing.

Refer to Chapter 1, Shorthand and Longhand Theory, for detailed information about power off longhand analog tests.

11 Potentiometers and Rheostats

Potentiometers and rheostats are variable resistance devices that require operator interaction to ensure that they are tested properly. Potentiometers, rheostats, and switches are tested as a section before the other passive analog devices to avoid guarding problems. The following illustration shows typical potentiometer (R3) and rheostat (R1) circuits. (Sample nodes are circled.)



Both potentiometers and rheostats are tested with essentially the same two techniques.

A potentiometer is usually examined in two pages of a single test step as a variable resistor with two independent resistances. For potentiometers, your program must ensure that a diagnostic message is not generated even if the measurement is outside the bounds defined by the stated tolerance. The first half of the test instructs the operator to center the potentiometer by testing for half of the potentiometer's value. After the potentiometer is adjusted, the tester checks the other half.

A rheostat test step measures the overall resistance value, then sets the variable output, or wiper arm, of the resistor to a predetermined value.

The two-terminal rheostat method ensures that the wiper arm is working properly and presets the output of the device, reducing calibration time during later assembly operations.

The rheostat program should instruct the operator to set the wiper arm of the rheostat to a fully counterclockwise position, then press the tabletop Start button to continue program execution. The program should check to ensure that the value of the rheostat is correct. If the rheostat passes the first part of this examination, instruct the test to repeat on a failure loop so the operator can adjust for some value, otherwise generate a failure message and skip the loop.

You can use Repeat to repeat the associated test until the operator presses the Start key. While Repeat is active (On), the display line is also enabled so that the operator can observe the measurement data. When the adjustment is complete, have the operator press the Start key to continue testing. Perform the measurement again after the operator presses the Start key to compare the measurement results against the test limits. The Repeat time field controls the rate of samples during the repeat loop. The tester waits the specified time before measuring.

Shorthand test accuracy is affected by the following factors:

- Shorthand accuracy tolerance
- System resistance, capacitance, or inductance (if not subtracted)
- Guard ratio error tolerance
- Device-under-test (DUT) tolerance

Test Step Editing

You can edit a potentiometer or rheostat test step at any time from the Step Worksheet. The Step Worksheet contains a menu bar, Component Properties, and Test Properties.

To open a potentiometer or rheostat Step Worksheet from the Main menu, select:

1. The board program
2. Edit
3. Passive
4. Switches/Pots...
5. A potentiometer ID or rheostat ID from the Component Select window

Component Properties

The Component Properties portion of the Step Worksheet for potentiometers and rheostats is the same as that for resistors. Refer to the Component Properties Editing section for resistors and for an explanation.The only difference will be the Device Type field, which will state either Potentiometer or Rheostat, depending on the type of device.

Refer to the **Z1800-Series Programmer's Guidebook**, Chapter 3, for general information about editing Component Properties.

Test Properties

Potentiometer and rheostat Test Properties contain the parameters to execute the test step. To edit Test Properties, select Edit from the Step Worksheet menu bar, then Test Properties—or, with a mouse, simply place the cursor on the Test Properties data field you wish to edit.

An example of a potentiometer and rheostat Step Worksheet with pop-up menus follows. Rheostat entries are shown in the following illustration in brackets and parentheses.

Beta
Cap Phase
CapScan
Capacitor
DigFuncProc
Diode
Discharge
External Program
IEEE
Inductor
No test
Resistor
Test I Stim V
Test I Stim V Stim V
Test V
Test V Stim I
Test V Stim I Stim V
Test V Stim V
Test V Stim V Stim V
Transistor
Zener

18xx Windows mode-init_com

Edit Options Tools Save Revert Validate Quit

Component Properties [↑]–[↓]

+ID:P1 (RR1) Name:11k (10k) Desc:Measure 10 to 1 tap Potentiometer
Value:11 Kohms (10Kohms) Device Type: **(Rheostat)**
Tol 1: 1 Number of Pins: 3 (2)

Test Properties [↑]–[↓]

Options: Pre Post Cntrl
Indicators
Current Page: Page 1 of 2

Test Type: **Resistor**

Test Data

Value : 10
Scale : Kohms
High : 11
Low : 9
Stim Val (mv):
Stimulus : Pin 1 (36) [Pin 1 (41)]
Measure : Pin 2 (68) [Pin 2 (68)]
Guard : 43 (No rheo guard)
Wait (ms) : 0
Squelch (ms) : 0

Controls

Wire Mode: 3 Precise: Off Averaging: 10
Fast Mode: Off Guard Mode: Active

C:\TPD\DEMO-ICT START CANCEL SOF HLD RPT CRT

Ohms
Kohms
Mohms
Default
6 decimal

APC
Analog template
Beta-NPN
Beta-NPN
CapScan
Capacitor
DigFuncProc
Diode
Discharge
Inductor
Potentiometer
Resistor
Rheostst
Rpack-DB
Rpack-DI
Rpack-DT
Rpack-SB
Rpack-SI
Rpack-ST
Transistor-NPN
Transistor-PnP
Zener

Test Data

Value : 1
Scale : Kohms
High : 1.1
Low : 0.9
Stim Val (mv):
Stimulus : Pin 2 (68)
Measure : Pin 3 (43)
Guard : 36
Wait (ms) : 0
Squelch (ms): 0

Page 2 of 2 changes for potentiometer.

Upper Test Properties Area

Field	**Description**
Test Type:	Type of test configuration used on current Step Worksheet. Recommended for inductors:
Resistor	Shorthand potentiometer test
Test I Stim V	Voltage stimulus and current measurement test
Test V Stim I	Current stimulus and voltage measurement test

Test Data/Middle Test Properties Area

Value	Numeric field specifying nominal expected value of Scale. Range = 0 – 999.
Scale:	Value field's unit modifier based on Test Type.
Resistor	Ohms, Kohms, Mohms
Test I Stim V	na, ua, ma
Test V Stim I	uv, mv, V

The Test Type field allows you to select an analog test configuration or test type to execute the step. Test types can be either shorthand or longhand. The shorthand Test Type for rheostats and potentiometers is Resistor. The longhand test types are Test V Stim I and Test I Stim V.

When you change test types, certain Test Properties fields also change, especially when changing from shorthand to longhand.

The following fields function the same for potentiometers and rheostats as they do for capacitors.

Refer to the **Z1800-Series Programmer's Guidebook**, Chapter 3, for more information about the following fields.

High and Low	Squelch
Stimulus	Wire Mode
Measure	Precise
Guard	Higuard
Wait	Averaging

12 RESISTORS

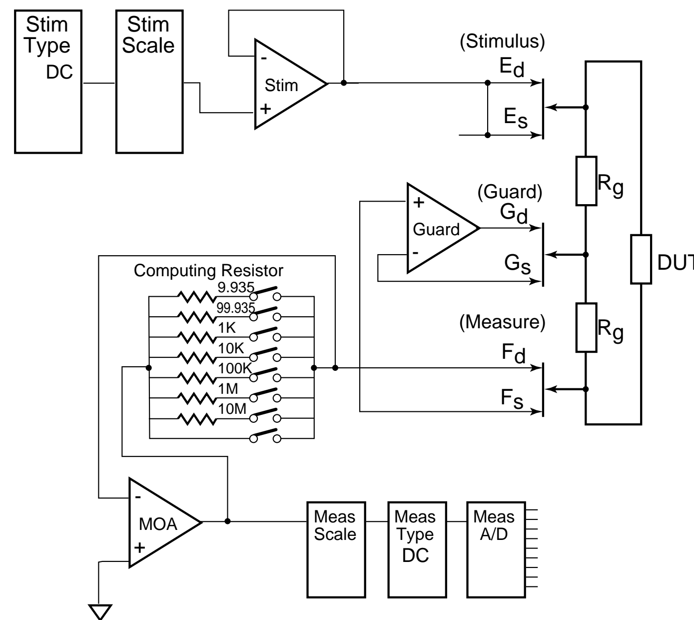
Resistor tests can be divided into two basic modes of testing—shorthand and longhand. The shorthand mode is a component-specific test that offers the best possible performance since the system software can automatically make certain assumptions and corrections.

The shorthand test is done through the Resistor Test Type. It can be further divided into standard resistor tests and extended resistor tests.

The PRISM-Z (PRecision Integrated Signal Measurement) module is available as an option and can be used for Resistor tests. Refer to the **Z1800-Series PRISM-Z User's Guide** for a complete discussion about the PRISM-Z test types available for Resistor tests.

Standard Resistor Test (Extended Off)

The following illustration shows a basic resistor shorthand test—3-wire, Precise of



Theory

The ATB is setup for Test I Stim V mode that places the DUT in the input leg of the measurement operation amplifier (MOA). The summing junction at the F pole is held at virtual ground by the output current of the MOA flowing through the selected computing resistor. The output voltage of the MOA is proportional to the impedance of the DUT and is routed via scale selectors to the A/D converter. Stimulus and measure types are always set to DC while the stimulus scale (stimulus voltage) depends on the expected value of the DUT. The Measure scale and computing resistor are chosen in order to yield the most accurate measurement. The stimulus voltage is normally set to 200 mv except for target DUT values above 2 MΩ where it is set to1 V and values above 20 MΩ where it is set to 10 V. Higher stimulus voltages can cause guarding problems. Use Extended Mode to control the stimulus voltage.

Test accuracy is affected by the following factors:

- Shorthand system accuracy
- System resistance if not in 5/6-wire mode, Precise
- Guard ratio error
- Device-under-test (DUT) tolerance

Refer also to page 5 for more information about Extended Mode.

Refer also to the Resistor Range and Accuracy table in the **Z1800-Series Maintenance Reference**.

Effects of system resistance

The Setup/Environment menu contains a field for system resistance with a default value of 1.5 Ohms. This value is subtracted for all shorthand resistor tests done in 3-Wire with Precise off. The 1.5 Ohm is merely an average and is not necessarily correct for all node combinations. For any other wire modes, or if Precise is enabled, the system resistance is corrected for by the measurement setup. Because of the increasingly unfavorable ratio between system and DUT resistance for component values below 200 Ohms, 5- or 6-Wire mode and/or Precise mode should be used to test such components. The greatest accuracy can be obtained in 5- or 6-Wire mode with Precise on.

Resistor Test Step Editing

You can edit a resistor test step at any time from the Step Worksheet. The Step Worksheet contains a menu bar, Component Properties, and Test Properties.

To open a resistor Step Worksheet from the Main menu, select

1. The board program
2. Edit
3. Passive
4. Resistors
5. A resistor ID (R2, for example) from the Component Select window

A typical resistor Step Worksheet appears below

Beta
Cap Phase
CapScan
Capacitor
DigFuncProc
Diode
Discharge
External Program
IEEE
Inductor
No test
Resistor
Test I Stim V
Test I Stim V Stim V
Test V
Test V Stim I
Test V Stim I Stim V
Test V Stim V
Test V Stim V Stim V
Transistor
Zener

18xx Windows mode-init_com

Edit Options Tools Save Revert Validate Quit

Component Properties [↑]-[↓]

+ID:R2 Name:100K Desc:

Device Type: **Resistor**
Number of Pins: 3

Test Properties [↑]-[↓]

Options: Pre Post Cntrl
Indicators
Current Page: Page 1 of 1

Test Type: **Transistor** Extended Off

Test Data

Value : 100
Scale : Kohms
High : 105
Low : 95
Stim Val (mv):
Stimulus : Pin 1 (36) [Pin 1 (41)]
Measure : Pin 2 (68) [Pin 2 (68)]
Guard : 43 (No rheo guard)
Wait (ms) : 0
Squelch (ms) : 0

Controls

Wire Mode:**4** Precise: Off Averaging: 10
Fast Mode: Off Guard Mode: Active

C:\TPD\DEMO-ICT START CANCEL SOF HLD RPT CRT

Ohms Default
Kohms 6 decimal
Mohms

3
4
5
6

APC
Analog template
Beta-NPN
Beta-NPN
CapScan
Capacitor
DigFuncProc
Diode
Discharge
Inductor
Potentiometer
Resistor
Rheostst
Rpack-DB
Rpack-DI
Rpack-DT
Rpack-SB
Rpack-SI
Rpack-ST
Transistor-NPN
Transistor-PnP
Zener

Component Properties Editing

Component Properties for resistor test operates as it does for analog tests in general.

Refer to the **Z1800-Series Programmer's Guidebook**, Chapter 3 for detailed information about Component Properties fields.

Resistor tolerance is symmetrical with the high tolerance and low tolerance being equal. Therefore resistor tolerance in Component Properties requires only one field.

If you wish to alter the testing limits, do not modify the resistor tolerance field in Component Properties. Instead use the Tolerance Calculator menu to change the testing limits in Test Properties.

To open the Tolerance Calculator:

1. In the worksheet, double-click the Value, High, or Low fields.

   The calculator shows the current worksheet values and tolerance. A field is available where you can modify the high and low tolerances. Another field shows how your modifications will effect the worksheet values.
2. Select OK to accept the values or Cancel to exit the Tolerance Calculator.

Test Properties Editing

Test Properties for resistor tests operates as it does for analog tests in general except for instances listed below in the table, Resistor Test Properties fields.

Refer to the **Z1800-Series Programmer's Guidebook**, Chapter 3 for detailed information about Test Properties fields.

Test Properties fields specific to resistor tests are described in the following table.

Upper Test Properties Area	
Field	**Description**
Test Type:	Type of test configuration used on current Step Worksheet. Recommended Types for resistors follow below:
Resistor	Shorthand resistor test.
Test I Stim V	Voltage stimulus and current measurement test. (Preferred for resistor test. See Chapter 1, Shorthand and Longhand Theory.)
Test V Stim I	Current stimulus and voltage measurement test.
Extended	Enables extended shorthand test. Default is Off.
Test Data/Middle Test Properties Area	
Value	A numeric field specifying the nominal expected value of Scale. Range = 0 – 1000.000
Scale	Value field's unit modifier based on Test Type.
Resistor	Ohms, Kohms, Mohms
Stim Val (mv)	A numeric field to specify stimulus value in mv. Range = -750–+750 mv DC. Default = 200 mv.
Controls/Lower Test Properties Area	
Fast Mode	ON or OFF. Default is OFF. When ON, test runs without built-in Wait and Squelch times.

Fast Mode. The Fast option when set to ON suppresses built-in wait and squelch times for improved throughput. Depending on the expected value of the DUT, the system normally supplies default squelch and wait times that might not be needed depending on the topology of the board. When you enable Fast Mode, you must find appropriate wait and squelch times yourself. While small wait times are often needed, squelch times are an issue only when the Higuard option is also selected.

Refer to the **Z1800-Series Programmer's Guidebook**, Chapter 5, for a discussion of Higuard, Wait and Squelch times, Wire Mode, and Precise.

Tools/Test Parameters

To see the actual low level test parameters for a particular shorthand resistor test, use the Test Parameters option from the Tools pull-down menu while the particular shorthand resistor test is displayed on the Step Worksheet.

Standard Resistor Test (Extended On)

As mentioned above, the stimulus voltage for regular shorthand test is set to 1 or 10 Volts for expected values above 2 Mohms in an attempt to improve the signal to noise ratio for these test. Unfortunately, the high stimulus voltage poses a problem when testing a DUT in the vicinity of semiconductors that start to conduct at a voltage of 0.7V and cause a guarding problem.

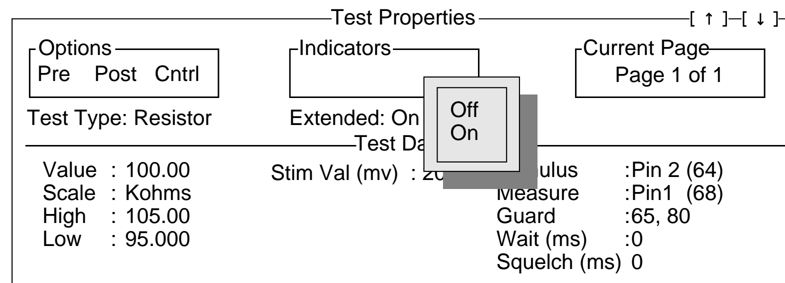
To overcome this problem, the shorthand resistor test has an Extended option. With it turned on, one can define the stimulus voltage and polarity. This facility enables one to override the high stimulus voltages and choose voltages low enough to prevent turning on surrounding semiconductors.Above is an example of semiconductor in parallel with a high impedance resistor. A regular shorthand resistor test would place the stimulus at node 1 and the measurement pole at node 119 to measure at the least loaded node for noise reduction. The regular ATB stimulus would then be -1 V in respect to the measurement pole. This, in turn, would introduce an unguardable path through the Base-Emitter connection of transistor T1. To alleviate the situation, you can either define a positive 1 V stimulus or one that is lower than -0.5 V. The first solution would eliminate the problem by reverse biasing the junction; the second solution would eliminate the unguardable path by not turning on the B-E semiconductor junction.

While regular shorthand resistor tests are bound to one range selected by the expected component value, extended mode tests perform autoranging in order to span wide tolerance request without degrading accuracy at either end. Autoranging makes it possible to create tests with a range of, for example, from 1 to 100 KΩ without the occurrence of overranging.

Extended Shorthand Test Editing

The extended shorthand mode uses all of the test page fields as described above in the shorthand test editing section plus two others: the Extended field and the Stim Val field.

The Extended field allows you to enable or disable the extended mode for resistor test. It is an On/Off field, with the default state being Off.



When the Extended field is in the On state, the Stim Val (Stimulus Value) field in the Test Data section of Test Properties is enabled, allowing you to specify the stimulus voltage in millivolts. The default is 200 mv, with a range of -750 to +750 millivolts.

Resistors in Parallel with other Components

When resistors are in parallel with capacitors, the program generator copies the resistor test into page one of a two-page capacitor test in the Capacitor section. The original resistor test in the resistor section is disabled but left in place for documentation purposes. The resistor test needs to be done with the best accuracy possible by using averaging, precise and wire mode controls since it directly affects the outcome of the capacitor reading. For large paralleling capacitor values, an increasingly large wait time needs to be programmed during the resistor test to let the parallel capacitor charge up before a measurement is taken.

See the Capacitor Test Type for more details on RC testing.

Resistors/Resistors

When resistors are in parallel with other resistors there is no way to electrically separate them. The only option is to measure the bulk impedance of the combination. The bulk impedance is calculated with the following formula:

$$\text{R total} = \frac{R1 \cdot R2}{R1 + R2}$$

where R total = Bulk impedance in Ohms
R1 = R1 impedance in Ohms
R2 = R2 impedance in Ohms

For more than 2 resistors the formula looks like this:

$$\frac{1}{\text{R_tot}} = \frac{1}{R1} + \frac{1}{R2} + \frac{1}{R3} + \frac{1}{Rn}$$

When resistors are in parallel with semiconductors, it is important to use extended mode to keep the stimulus voltage below the semiconductor turn-on voltage of 0.7 V. Programing for stimulus values of less than 500 mv, generally prevents any semiconductors from conducting.

See also the discussion for Extended mode.

Longhand Testing of Resistors

Resistors can also be tested by using longhand Test Types TISV and TVSI. These test types are programmed in generic units of volts and amperes. Because the diagnostic messages produced for longhand tests are not based on DUT units of Ohms, failure diagnostics are hard to interpret.

Refer to Chapter 1, Shorthand and Longhand Theory, for a complete discussion of shorthand and longhand testing.

13 Rpacks

Resistor packs (Rpacks) are tested as multipage resistors. Refer to the Resistor Tests section for details regarding standard resistor test methods and Test Properties fields.

The Tol field for Rpacks is symmetric; that is, the low value tolerance is the same as the high value tolerance. Do not use this field to alter test limits. Alter test limits either in Test Properties, with the tolerance calculator, or by direct entry of high and low limits.

The Device Type field offers the following choices for Rpack testing:

RPACK-DB	Dual bus
RPACK-DI	Dual in-line
RPACK-DT	Dual terminator
RPACK-SB	Single bus
RPACK-SI	Single in-line
RPACK-ST	Single terminator

Refer to the **Z1800-Series Programmer's Guidebook**, Chapter 8, for illustrations of these Rpack types.

The Number of Pins field defines the test generation process for the test step and configures the Node Entry window with the correct number of pins. This field defines the number of pins on the device to which tester nodes will be connected. For Rpacks, enter as many as apply to the package type.

Rpack Test Step Editing

You can edit an Rpack test step at any time from the Step Worksheet. The Step Worksheet contains a menu bar, Component Properties, and Test Properties.

To access an Rpack Step Worksheet from the Main menu, select:

1. Edit
2. Passive
3. Rpacks
4. The Rpack ID from the Component Select window.

Rpacks are multipage resistor tests. To move through the pages, click the up or down arrows in Test Properties.

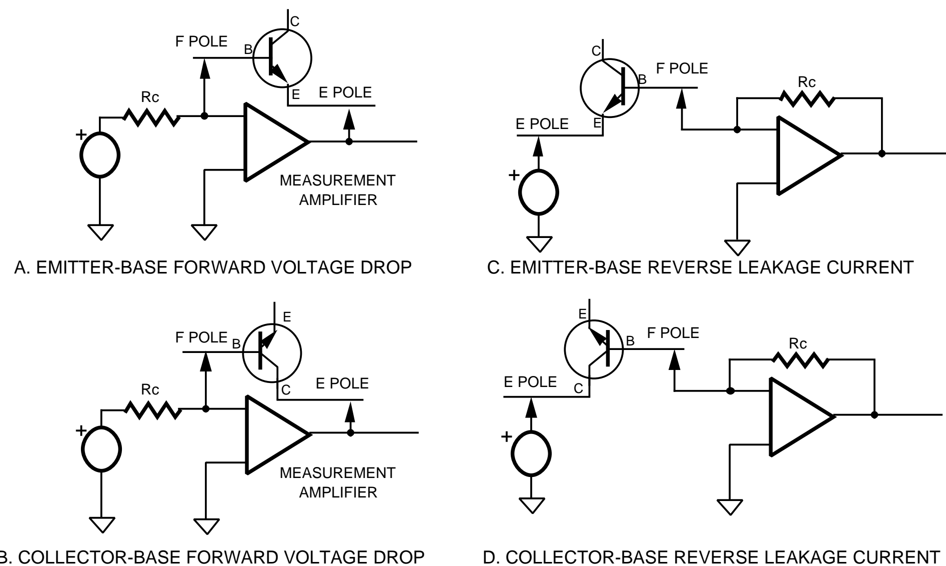
14 Transistor and Gain

Transistors are tested as two back-to-back diodes. Because transistors have two junctions, two Test Properties pages are required—one for an emitter-base (E-B) diode test and one for a collector-base (C-B) test.

For PNP transistors, the anodes of the diode tests are the collector and emitter. For NPN transistors, the anodes are the base. Each Test Properties page (diode test) will measure a forward voltage drop in response to an injected forward current, and an optional reverse (leakage) current measure in response to an applied reverse voltage.

The figure below illustrates the equivalent circuit configurations for both NPN and PNP transistors. The forward voltage drop test places the transistor in the feedback loop of the measurement amplifier circuit. Reverse leakage tests place the transistor between the stimulus and the input to the measurement amplifier.

Transistor test circuit configuration diagram.



Testing Techniques

Transistors with parallel semiconductor junctions or unguardable parallel paths are usually examined for proper orientation only.

Transistor junctions with parallel unguardable resistors can be examined using the shorthand NPN or PNP statements; however, the measurement values must be modified to compensate for the effects of the resistor. The test is possible because the transistor junction exhibits different resistance values depending on whether the junction is forward-biased or reverse-biased.

The forward voltage drop is usually lower because of current flow through both the resistor and the transistor junction. To compensate for current loss in the parallel component, the Forward Current (ma) can be increased to achieve the proper forward drop voltage across the transistor junction. The reverse leakage current usually cannot be tested.

Unguardable parallel capacitors do not usually influence transistor junction measurements. A delay (wait state) can be added in parallel between stimulus application and measurement execution so the capacitor can be charged to eliminate the capacitor current from the transistor measurement.

Field Effect Transistors

Like NPN or PNP transistors, which can be lumped into broad categories allowing generalized stimulus and measurement parameters, FETs can also be lumped into two broad categories: JFETs, junction field effect transistors, and IGFETs, insulated gate field effect transistors.

There are many kinds of JFETs and IGFETs, each with different parameters for voltage and current. Almost every device on the tested assembly must be individually examined and the unique stimulus and measurement values empirically determined. FETs are also more sensitive to the components surrounding the printed circuit board assembly than NPN and PNP transistors.

Test V Stim I is normally used to test FETs while they are in the on state. The gate electrode is guarded, forcing the device to switch on. The F pole is connected to the drain electrode, keeping it essentially at zero volts or virtual ground. The E pole is connected to the source lead.

An appropriate current I_c is applied to the drain electrode and the response voltage measured. Since the JFET is essentially turned on, the expected response voltage should be close to zero volts. A typical JFET source-drain voltage drop is approximately 0.3 volts.

The stimulus current required to force the source-drain voltage drop to zero volts varies widely depending on the characteristics of the tested device. Values of I_c may vary between 0.1 mA and 1.0 mA, with the acceptable stimulus value discovered during the programming debugging process.

Acceptance limits also depend on the characteristics of the particular device-under-test. Generally, a source-drain voltage greater than 0.5 volts indicates a defective device.

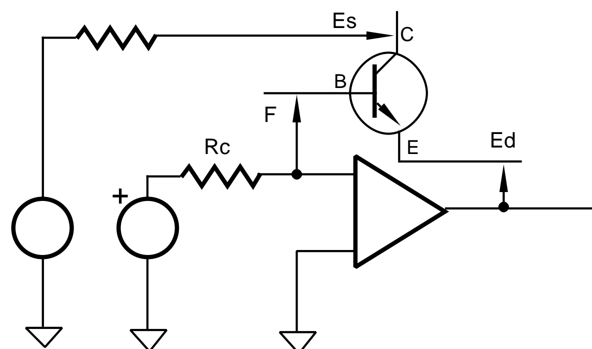
Dual stimulus tests can be used to create a switch on test for active components.

Reversed Transistors and Beta Test

One of the more common assembly errors found on printed circuit boards is reversed transistors. A 180° rotation of these transistors causes the collector and the emitter to exchange positions. Assembly reversal will allow a transistor to pass the standard transistor test that checks for the existence of back-to-back diodes. If product history indicates a reversed transistor problem, use the Beta (Gain) test to discover errors before board power is applied.

The Beta test requires special fixture wiring and node placement considerations to account for two stimulus sources. The emitter must be on analog drive poles. The collector must be on an analog sense pole. The first 16 nodes on every driver/receiver board are on the analog drive pole. The second 16 nodes are on the analog sense pole.

The Beta test configuration appears below.



Transistor Test Step Editing

You can edit a transistor test step at any time from the Step Worksheet. The Step Worksheet contains a menu, Component Properties, and Test Properties.

To access a transistor Step Worksheet from the Main menu, select:

1. The board program
2. Edit
3. Semi
4. Transistors
5. A transistor ID (Q1, for example), from the Component Select window.

Component Properties Editing

Refer to the **Z1800-Series Programmer's Guidebook**, Chapter 3, for a description of Component Properties fields.

Transistors, however, do not have value or tolerance fields because the reverse voltage test values are predetermined by the software and reported in Test Properties High and Low fields.

Test Properties Editing

To edit a transistor Test Properties, select Edit from the menu bar, then Test Properties—or simply place the cursor on the data field you wish to edit. An example of a transistor Step Worksheet with pop-up menus appears below.

APC Resistor
Analog template Rheostst
Beta-NPN Rpack-DB
Beta-PNP Rpack-DI
CapScan Rpack-DT
Capacitor Rpack-SB
DigFuncProc Rpack-SI
Diode Rpack-ST
Discharge **Transistor-NPN**
Inductor Transistor-PnP
Potentiometer Zener

18xx Windows mode-init_com
Edit Options Tools Save Revert Validate Quit
Component Properties [↑]–[↓]
+ID: Q1B Name: 2222A Desc: NPN-Gain
Gain:120 Coll Curr: 0.000 **ma** Device Type: **Transistor-NPN**
Number of Pins: 3
Test Properties [↑]–[↓]
Options: Pre Post Cntrl
Indicators
Current Page
Test Type: **Transistor**
Test Data
Scale: mv
High : 840
Low : 560
Forward Curr (ma) : 10.000
Reverse Test : **Yes**
Reverse Curr (ua) : 1
Stim Node On : **PNP-B/E**
Stimulus : Pin 2 (1)
Measure : Pin 1 (9)
Guard :
Wait (ms) : 0
Squelch (ms) : 0
Controls
Wire Mode: 3 Precise: Off Averaging: 1
Guard Mode: Active
C:\TPD\DEMO-ICT START CANCEL SOF HLD RPT CRT

uv Default
mv 6 decimal
V

No
Yes

PNP-B/E
PNP-E/B
PNP-B/C
PNP-C/B
NPN-E/B
NPN-B/E
NPN-C/B
NPN-B/C

Beta **Resistor (Prism)**
Cap Phase Test I Stim V
CapScan Test I Stim V (Prism)
Capacitor Test I Stim V Stim V
Capacitor (Prism) Test V
DigFuncProc Test V (Prism)
Diode Test V Stim I
Discharge Test V Stim V (Prism)
External Program Test V Stim I Stim V
IEEE Test V Stim V
Inductor Test V Stim V (Prism)
Inductor (Prism) Test V Stim V Stim V
No.Test Transistor
Resistor Zener

The following table describes the fields unique to transistor test. Transistor tests generally have 3 pins contained on 2 Test Properties pages.

Refer to the **Z1800-Series Programmer's Guidebook**, Chapter 3, for further information about the Test Properties fields.

Upper Test Properties Area

Field	**Description**
Test Type:	The type of test configuration used on the current Test Properties page.
Transistor	Shorthand transistor test
Beta	Beta (gain) shorthand test. (See the following table.)
Test I Stim V	Voltage stimulus and current measurement test. (See Longhand Analog section)
Test V Stim I	Current stimulus and voltage measurement test. (See Longhand Analog section)

Test Data/Middle Test Properties Area

Scale (Transistor Test Type)	uv, mv, V
Forward Current (ma)	Adjustable current value. Default 10 (ma)
Reverse Test	YES or NO. When YES, performs reverse leakage test.
Reverse Curr (ua)	When Reverse Test is YES, enter number from 0 to 999 (ua).
Stim Node On	Anode or Cathode stim pole connection, to adjust polarity of forward drop and reverse leakage tests. Choices for NPN and PNP are: E/B–emitter/base (stim node on emitter); B/E–base/emitter (stim node on base); C/B–collector/base (stim node on collector); and B/C–base/collector (stim node on base).

An example of a transistor Beta Step Worksheet with pop-up menus appears below.

APC | Resistor
Analog template | Rheostst
Beta-NPN | Rpack-DB
Beta-PNP | Rpack-DI
CapScan | Rpack-DT
Capacitor | Rpack-SB
DigFuncProc | Rpack-SI
Diode | Rpack-ST
Discharge | Transistor-NPN
Inductor | Transistor-PnP
Potentiometer | Zener

ma
A

18xx Windows mode-init_com

Edit Options Tools Save Revert Validate Quit

Component Properties [↑] [↓]

+ID: Q1B Name: 2222A Desc: NPN-Gain

Gain:120 Coll Curr: 0.000 **ma** Device Type: **Beta-NPN**
Number of Pins: 3

Test Properties [↑] [↓]

Options: Pre Post Cntrl | Indicators | Current Page

Test Type: **Beta**

Test Data

Gain : 120.000 | Collector Current : 10 | Emitter : Pin 2 (1)
Transisitor : **NPN** | Scale : **ma** | Base : Pin 1 (9)
: | Wait (ms) : 0 | Collector : Pin 3 (68)
| Squelch (ms) : 0 | Guard :

Controls

Wire Mode: 3 | Precise: Off | Averaging: 1
Guard Mode: Active

C:\TPD\DEMO-ICT START CANCEL SOF HLD RPT CRT

PNP
NPN

na
ua
ma

Beta | Resistor (Prism)
Cap Phase | Test I Stim V
CapScan | Test I Stim V (Prism)
Capacitor | Test I Stim V Stim V
Capacitor (Prism) | Test V
DigFuncProc | Test V (Prism)
Diode | Test V Stim I
Discharge | Test V Stim V (Prism)
External Program | Test V Stim I Stim V
IEEE | Test V Stim V
Inductor | Test V Stim V (Prism)
Inductor (Prism) | Test V Stim V Stim V
No.Test | Transistor
Resistor | Zener

The following table describes the fields unique to Beta test.

Refer to the **Z1800-Series Programmer's Guidebook**, Chapter 3, for further information about the Test Properties fields.

Upper Test Properties Area

Field	Description
Test Type: Beta	The type of test configuration used on the current Test Properties page. Beta (gain) shorthand test
Test Data/Middle Test Properties Area	
Gain	Minimum acceptable gain for beta transistor measurement.
Transistor	NPN or PNP
Collector Current	Amount of beta collector current. Used with Gain to compute base current.
Scale	na, ua, ma.
Wait (ms)	0 to 32000 ms. Added to default wait of 3 ms typical.
Squelch (ms)	0 to 32000 ms. Repeatable initial condition to remove stored energy.
Emitter	Emitter pin/node number.
Base	Base pin/node number.
Collector	Collector pin/node number.
Guard	Pin/node number(s) of the guard point(s). 10 nodes max.

The Beta test type uses both DC stimulus sources on the ATB to perform a beta measurement. One source is a constant voltage source on the collector, and the other a constant current source on the base of the transistor.

You must specify the desired operating collector current in the Collector Current field from transistor specifications (found in data books), so the transistor is in the middle of its operating range, instead of at the saturation or cutoff point.

You must also specify the minimum acceptable gain or Hfe in the Gain field. This field is the minimum acceptable passing value.

Given the two inputs, I_c (desired Collector Current), and Hfe (Gain), the tester computes the required I_b base current. The tester also selects the required stimulus voltages and computing resistors for proper operation. The tester chooses values that put the collector-to-emitter voltage at approximately 3 volts.

With I_b applied and V measure sampled, the tester computes I_c. The tester will make up to 20 adjustment attempts, incrementing I_b base current each time until the I_c is approximately the requested I_c. The tester will increment in 20% positive and 10% negative steps until it homes in on the requested Ic within a 5% of the requested Ic.

The tester takes a final measurement calculates the gain.

The Gain field represents the minimum acceptable gain for measurement on a transistor device.

The Transistor field specifies whether the device is a PNP or NPN type of transistor. This information configures the test connections and stimulus polarities.

The Collector Current field allows you to specify the amount of collector current before the tester computes the gain measurement. In other words, this entry specifies the gain measurement

operating point. With this value, plus the value in the Gain field, the tester computes the base current for the test.

The Emitter field indicates the node number that connects to the transistor's emitter. If you automatically generate the program, the software completes the field. You can also edit this field.

The Base field indicates the node number that connects to the base of the transistor.

The Collector field indicates the node number that connects to the collector of the transistor.

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