Z1800-Series

MultiScan User's Guide

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Z1800-SERIES MULTISCAN USER'S GUIDE

Manual History

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Version A.0 DeltaScan software and Version B.0 FrameScan/WaveScan software for use with F.0 operating system.
Supersedes *WaveScan User's Guide* (Version A.0 for use with E.4 operating system) and preliminary edition of *DeltaScan User's Guide*.

Additional copies of this manual may be obtained from Teradyne.

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PREFACE

MultiScan Package

The **MultiScan** package includes five power-off test techniques for use with Teradyne's popular Z1800-series board testers: DeltaScan, WaveScan, FrameScan, FrameScan Plus, and CapScan. This manual devotes a separate chapter to each technique.

The five MultiScan tools provide complementary approaches to testing, yielding power-off, vectorless test coverage for a wide variety of devices.The chapters covering the different techniques give details of their various procedures and requirements.

DeltaScan

DeltaScan detects opens on devices and broken bond-wires, and may detect "blown" input or output transistors or incorrectly oriented devices. DeltaScan can be employed without knowledge of the internal functioning of the device-under-test (DUT); however, it requires the DUT to have protection diodes and a substrate resistance to the ground pins.

WaveScan

WaveScan detects opens on device leads. It also detects broken bond-wires, and may detect "blown" input or output transistors or incorrectly oriented devices. It uses magnetic inducers mounted over the DUT; an oscillating magnetic field induces voltages in conducting paths in the DUT, verifying proper connection.

FrameScan

FrameScan detects opens on device leads. It also finds opens on socket or connector pins without making physical contact with the connector. FrameScan uses electrostatic inducers mounted over the DUT to capacitively couple signals into devices; the detected signal levels verify proper or improper connection.

FrameScan Plus

FrameScan Plus detects opens on device leads. It uses sensors mounted over the DUT to detect capacitively coupled signals from devices; the detected signal levels verify proper or improper connection.

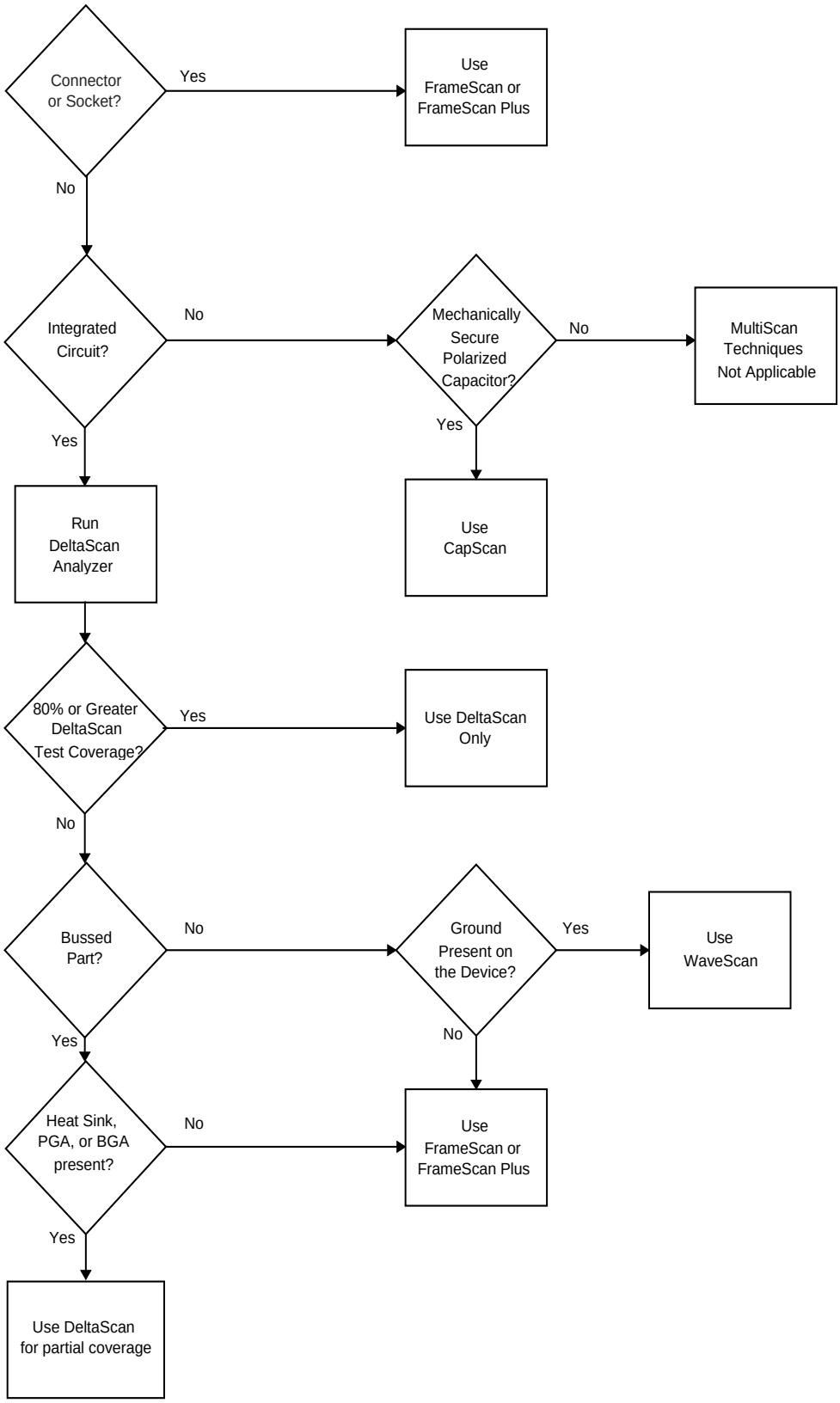
CapScan

CapScan detects incorrect orientation of polarized capacitors. CapScan uses sensors mounted over the capacitor to compare relative detected signals driving each lead of a polarized capacitor, verifying the device orientation.

MultiScan Flowchart

The flowchart that follows may help you decide which MultiScan technique you should use for testing a particular device; more detailed charts for DeltaScan, WaveScan, FrameScan, and FrameScan Plus appear in the chapters covering each technique.

Note: More detailed flowcharts for choosing a MultiScan technique appear in the chapters covering DeltaScan, WaveScan, FrameScan, and FrameScan Plus.


Connector or Socket?
Yes
Use FrameScan or FrameScan Plus
No
Integrated Circuit?
No
Mechanically Secure Polarized Capacitor?
No
MultiScan Techniques Not Applicable
Yes
Use CapScan
Yes
Run DeltaScan Analyzer
80% or Greater DeltaScan Test Coverage?
Yes
Use DeltaScan Only
No
Bussed Part?
No
Ground Present on the Device?
Yes
Use WaveScan
No
Yes
Heat Sink, PGA, or BGA present?
No
Use FrameScan or FrameScan Plus
Yes
Use DeltaScan for partial coverage

CHAPTER 1 DELTASCAN

DeltaScan is a power-off, digital test technique that provides vectorless tests to detect opens on devices for Z1800-Series board testers. DeltaScan also detects broken bond-wires and poor solder connections, and may detect “blown” input or output transistors and mis-oriented devices.

DeltaScan can be used without knowledge of the internal functioning of the device under test (DUT); however, it does require that the DUT has parasitic protection diodes and a substrate resistance to the ground pin.

DeltaScan automatically generates high pin-fault coverage tests. All DeltaScan tests have diagnosis “to the pin.”

DeltaScan is intended for verification of correct board assembly rather than detection of functional defects in the device.

Theory of Operation

DeltaScan works with two pins at a time, not counting ground. This is referred to as a pin-pair. DeltaScan takes two current measurements. The Delta is the difference between them. DeltaScan uses one pin as the stimulus pin, a second pin as a measurement pin, and another as a ground. Both the stimulus and measurement pin connections are verified if the delta is higher than the established threshold limit.

DeltaScan attempts several tests on a single pin before declaring a failure on the pin.

By analyzing board topology, DeltaScan excludes parallel paths that could cause false passes of device opens during testing. See “Analyze the Topology Report” on page 1-22. For details on managing topology, see Chapter 7, “Program Generator Tools” in the **Z1800-Series Programmer’s Guidebook.**

- **To measure the Delta:**

Note: As you read through the following steps, refer to the illustration below to see what happens inside a chip during a DeltaScan operation after node connections are made and DeltaScan is given the command to test a pin pair. Think of the diodes in the illustration as “ideal,” that is, current flow can only travel to ground.

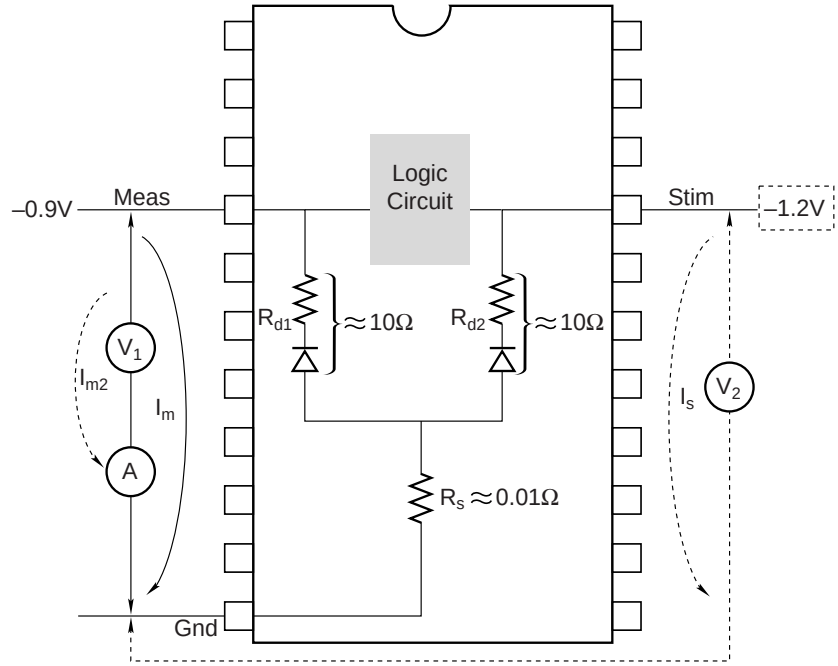
1 The system applies -0.9 V to the measurement pin and measures I_m as $-0.9\,V/(R_{d1} + R_s)$.

This results in decreased voltage across R_{d1}, causing the new current going into the measurement pin I_{m2} to be smaller than the original current I_m.

2 The system applies -1.2 V to the stimulus pin, causing additional current Is to flow through R_s, increasing the voltage across R_s.

The Delta is the difference between I_m and I_{m2}.

Values shown are for illustration purposes only.



KEY TO DIAGRAM

R_{d1}	Resistor diode 1
R_{d2}	Resistor diode 2
R_s	Resistor substrate
I_m	Measure current
I_s	Stim current
I_{m2}	New measure current
I_{Rs}	Current on substrate resistance
——	Step 1
- - - -	Step 2

Delta Measurement Formulas

First measurement:

$$I_m = \frac{V_1}{(R_{d1} + R_s)}$$

After stimulus voltage is applied, I_m becomes I_{m2} :

$$I_{Rs} = I_{m2} + Istim$$

$$V_1 = I_{m2} \times R_{d1} + I_{Rs} \times R_s$$

Or:

$$V_1 = I_{m2} \times R_{d1} + (I_{m2} + I_s) \times R_s = I_{m2} \times R_{d1} + I_{m2} \times R_s + I_s \times R_s$$

Solving for I_{m2} :

$$I_{m2} = \frac{(V_1 - I_s \times R_s)}{(R_{d1} + R_s)} = \frac{V_1}{(R_{d1} + R_s)} - \frac{I_s R_s}{(R_{d1} + R_s)}$$

Lastly:

$$\Delta I_m = I_m - I_{m2} = \frac{V_1}{R_{d1} + R_s} - \frac{V_1}{R_{d1} + R_s} + \frac{I_s R_s}{R_{d1} + R_s} = \frac{I_s R_s}{R_{d1} + R_s}$$

DeltaScan Hardware

DeltaScan hardware consists of a circuit board and two cables mounted in the test system. No fixture hardware is required, though some specific fixture wiring is needed to support DeltaScan. DeltaScan can be operated with either the VP or the THC board.

DeltaScan also includes two DC voltage sources (one for stimulus and one for measure), a differential ammeter (for measuring the measure current), and relays for connecting the DUT ground and all DUT power supplies to DeltaScan's ground.

The DeltaScan II board also provides control logic and power for the FrameScan Plus Selector Board. See Chapter 4 for information about FrameScan Plus.

- **DeltaScan Board**

  The DeltaScan board provides measurement, stimulus, and ground connections to the DUT. The DeltaScan board connects to the backplane to have access to power and the analog poles.
- **Cables**

  DeltaScan cables are:
  - Control cable, PN 047-246-XX (20, 40, or 60)
  - Fixture/receiver cable
- **Fixture Wiring**

  Most Z1800-Series testers shipped before 1995 must have 15 wires added to J2 of the fixture receiver in order to use DeltaScan. The DeltaScan option includes these wires as PN 046-492-00. For information about DeltaScan and fixture wiring, see the **Z1800-Series Fixturing Guidebook**.

DeltaScan Control

DeltaScan is controlled via the I/O Adapter PN 045-454-00, or Channel I/O board PN 045-456-00. It requires one of these two 16-bit I/O boards, and won't work with the older 8-bit PCIO boards, PN 045-030-00.

Hardware Installation

The DeltaScan board can be installed in either a spare slot or any driver/receiver (D/R) slot. Teradyne recommends installing the DeltaScan board in a spare slot if one is available.

Note: When the DeltaScan board is installed in a D/R slot, the D/R configuration reports the slot as empty.

The jumper on the DeltaScan board must match the position of the jumper on the I/O boards mentioned in "DeltaScan Control" below. "On" for THC revision S.0 or earlier; "Off" for VP and THC revision T.0 or later.

To connect the DeltaScan board, refer to the installation instructions provided with the hardware. For information on running the DeltaScan self-test, refer to the diagnostic chapter in the **Z1800-Series Maintenance Reference.**

DeltaScan Software

DeltaScan software consists of the following files:

- **DSCAN.EXE**—DeltaScan's executable file, supporting Test, Edit, and Validate operations; called from the 18xx operating system.
- **DTRAN.EXE**—Executable file called by 18xx program generator to create a DeltaScan database and update topology; can also be called from the MS-DOS command line to generate an ASCII version of a DeltaScan database and a DeltaScan analysis report from an input list.
- **DS_CONV.EXE**—Executable called from the 18xx operating system; converts a DeltaScan database from E.4 compatibility to F.x compatibility and provides links to the F.x test program.
- **ANALYZE.BAT**—A batch file that invokes DTRAN.EXE and allows for repeated analyze/edit cycles; used to correct syntax problems.

Software Installation

You should be familiar with the Z1800-Series tester hardware and software, including the directory structure.

- **To install DeltaScan using the DOS install:**

  1. Put the DeltaScan installation disk into your disk drive.
  2. Change to that drive by typing either **a:** or **b:** (drive A or drive B).
  3. Press **Enter**.
  4. Type: **install**
  5. Press **Enter**.
  6. Follow any instructions that appear on screen.

     DeltaScan files are copied to the \MOS directory of the tester where all the 18xx system files are located.

- **To install DeltaScan using the Windows install:**

  1. Put the DeltaScan installation disk into your disk drive.
  2. Click **Start** and select **Run**.
  3. Type either **a:setup** or **b:setup** (drive A or drive B).
  4. Press **Enter**.
  5. Follow any instructions that appear on screen.

     DeltaScan files are copied to the \MOS directory of the tester where all the 18xx system files are located.

When to Use DeltaScan

DeltaScan detects opens on digital devices, but can also detect broken bond-wires, and may detect “blown” input or output transistors or misoriented devices, as well as some cold solder joints. It can be employed without knowledge of the internal functioning of the DUT, but it is essential that the DUT has protection or parasitic diodes on the input and output pins, and a substrate resistance.

DeltaScan requirements make it less effective than other methods for testing connectors, devices lacking diodes, and devices lacking paths. In addition, it has only limited effectiveness testing devices lacking ground or bussed parts, and devices that analysis shows as lacking Proximity or Pairs.

The flowchart on the next page shows you how to determine whether DeltaScan is appropriate for testing a particular device. Key to this determination is the test coverage analysis that predicts the percent of coverage using DeltaScan techniques.

Test Coverage Analysis

The ANALYZE.BAT tool predicts DeltaScan test coverage and thereby, the appropriateness of DeltaScan testing for a particular device. ANALYZE.BAT calls the DTRAN.EXE analysis program and facilitates the editing of the IPL.DAT file if necessary. The analysis is based on information from the board input list.

The board input list (IPL.DAT) contains descriptions of board component parts and interconnections. Power, ground, and component data in the IPL must be accurate and complete for the coverage report to be useful. Digital components must be represented in the input list, but you do not need DSCAN tokens for the analysis.

- **To predict DeltaScan coverage:**

1. Use the Utility “**Dos Shell**” command to open an MS-DOS window.
2. At the MS-DOS prompt, type: **ANALYZE IPLFILE.DAT REPORT.TXT**

   where IPLFILE.DAT is the name of the source data file and REPORT.TXT is the desired name of the output file.

   or type: **ANALYZE IPL.LST REPORT.TXT**

   (if your IPL.LST is more current than your IPL.DAT).

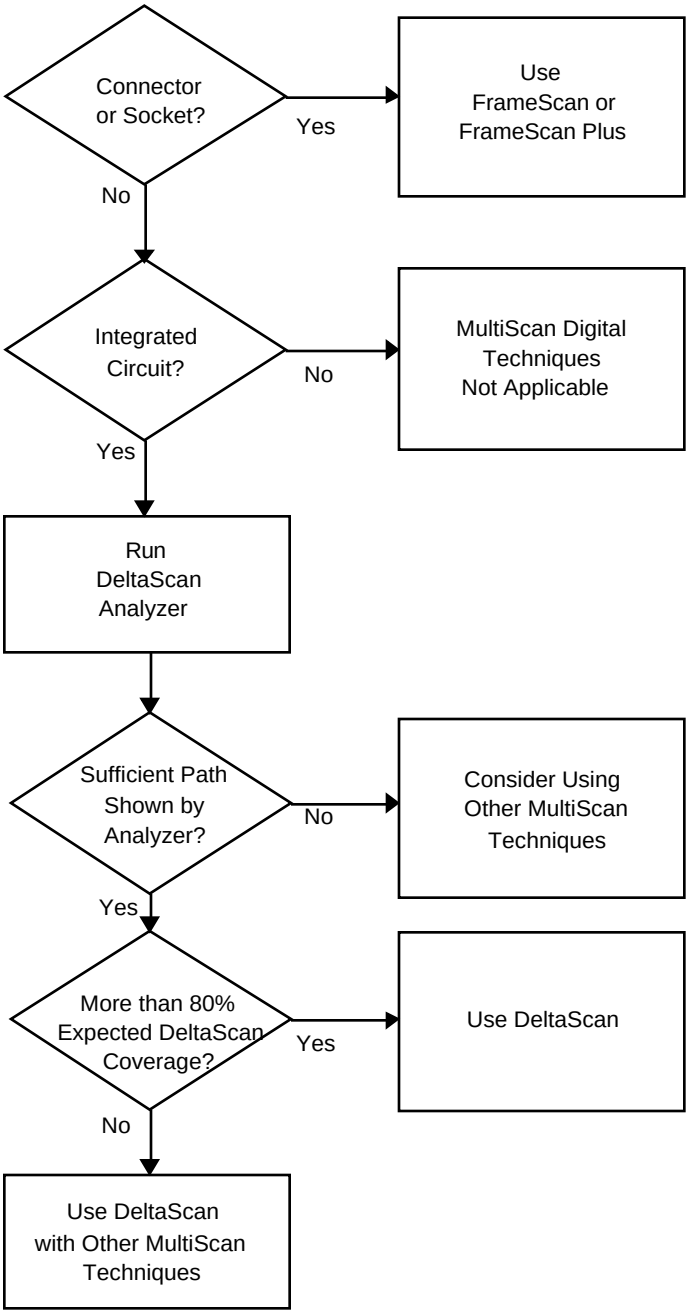
   DTRAN.EXE analyzes the IPL file and generates an ASCII report file. If DTRAN.EXE finds an error in the IPL, the system prompts for editing before completing the analysis.

   If you need to edit the IPL, press the Y(es) key. Make the necessary edits, and exit the editor.
3. When DTRAN.EXE has finished creating the output file, open it and check the coverage analysis.

Note: DTRAN.EXE does not require DSCAN tokens to appear in the input file. If you decide to develop DeltaScan tests after examining the analysis results, you must manually add DSCAN tokens to the IPL.

This flowchart shows how to determine whether DeltaScan is the appropriate testing strategy.

The ANALYZE.BAT tool predicts test coverage.



Analysis Report

The test coverage analysis looks at four topological attributes, Paths, Pairs, Proximity and Grounds, and scores each device between 0 and 100% for each of these attributes. These four scores are then combined to create a final, cumulative weighting for the device. They appear in the report file with one attribute per column, as shown below.

ID	Paths	Prox	Pairs	Gnds	Cumulative
IC102:	43%	100%	33%	100%	33%

The final weighting is performed according to the equation:

Cumulative total = (Paths / 3) x Pairs
+ (Paths / 3) x Proximity
+ (Paths / 3) x Grounds

The **maximum** figure given by paths is reduced by a weighting given to each of the other three attributes. Cumulative total is the **minimum** predicted coverage.

Topological Attributes

- **Paths**

  The Paths value is the percentage of pins on the device that have valid test paths (excluding no-connects and ground/power pins). This value represents the maximum coverage that could be obtained by DeltaScan.

- **Pairs**

  The Pairs value is the percentage of possible pin-pairs available for each pin on the device (excluding no-connects and ground/power pins). During Validate, DeltaScan attempts to create a database containing up to six tests for each pin, and this analysis quantifies how well that might be achieved. If a pin has three possible pin-pairs, then that pin scores 50%. The figure listed in this column is the summation of the pin-pairs on all of the pins on this device.

- **Proximity (PROX)**

  The further apart pin-pairs are, the less effective they often become. This figure calculates the average pin-pair separation distance for each of the first six possible pin-pairs on each pin, and creates a final weighting for the device.

- **Grounds**

  DeltaScan works by detecting common resistance to ground between pairs of pins. Current flows from each pin of the pair to ground, and where the current flow is through a common substrate, a common resistance is seen.

  If current flows from each pin to a different ground pin, or if the pins of the pair are positioned with a ground pin between them, there is not much common current, and hence not much common resistance. Common current flow is blocked by an intervening ground pin. This analysis weights each of the first six possible pin-pairs with a 1 or a 0 according to whether it is blocked or not. The number given is a summation of all of the pins on the device.

Component Prediction Details For each component, there is a listing of the possible pin pairing. For example:

```
Device: IC1
Name: 74LS169
Description: E45
Pin count: 16
Potential pin coverage: 100%

Pin  Node  Type      Nearest stim-pins
-----------------------------------------------------
 1    12  Normal    [15 2 14 3 13 4]
 2     5  Normal    [1 3 15 4 14 5]
 3    11  Normal    [2 4 1 5 15 6]
 4     4  Normal    [3 5 2 6 1 15]
 5    10  Normal    [4 6 3 2 1 15]
 6     3  Normal    [5 4 3 2 10 1]
 7  9999  N/C
 8   100  Gnd
 9    23  Normal    [13 15 12 1 11 2]
10     1  Normal    [11 12 13 6 14 5]
11     9  Normal    [10 12 13 14 15 6]
12     0  Normal    [11 13 10 14 15 1]
13     8  Normal    [12 14 11 15 10 1]
14    18  Normal    [15 12 11 15 10 1]
15    19  Normal    [13 12 14 11 10 1]
16   100  Pwr
```

In this example, the fields have the following meaning:

- **Device, Name, Description, Pin count, Potential pin coverage**

  Device, Name, Description, and Pin-count all have the same meaning as in all 18xx worksheets. Potential pin coverage is the maximum coverage extracted from the analysis data displayed above.

- **Pin, Node, Type, and Nearest stim-pins**

  The columns headed Pin, Node, Type, and Nearest stim-pins describe the first six possible pin-pairings that could be used during validate, and are the pairs which are used to derive the analysis data.

  Pin is the measurement pin.

  Type indicates the category into which this pin has been allocated for DeltaScan tests.

  - **Normal**–Pin has at least one test pair
  - **N/C**–Pin is not connected
  - **Pwr**–Pin is connected to power or power-bus
  - **Gnd**–Pin is connected to ground
  - **Tied Pwr**–Pin is tied to power or power-bus through a low impedance component.
  - **Tied Gnd**–Pin tied to ground through low impedance component.
  - **No path**–There are no pin pairs for this pin.
  - **Tied**–Pin is tied to another pin on this device.
  - **No Drive**–Pin is connected to a net which is too low in impedance for DeltaScan to drive.
  - **Meas Only**–Pin is connected to a net which is too low in impedance for DeltaScan to drive a stim-pin, but it can be driven as a meas-pin.

Note: An excessive number of TiedPwr, TiedGnd, or No-Drive nodes may indicate incorrect power definition. For example, if the power supply to the board was distributed through an inductor, this would be indicated as TiedPwr rather than Pwr. In this case, a wire to a DS Relay should be used to ground the output side of the inductor during DeltaScan tests, and the node should be entered into the IPL as a Power-bus (PB) token.

Link and Leak Data DeltaScan generates pin-pairing information from the IPL file by processing IPL data into two related categories, link and leak data. This information is displayed after the analysis so you can trace the cause of any unexpected results.

- **Link Data**

  Link data (jumper) describes the interconnects that DeltaScan found in board topology. At least two columns appear in the analysis report for all nodes that are not type Normal.

  The link data must have some power and ground nodes, otherwise DeltaScan cannot generate valid tests. Missing power and ground nodes indicate missing power steps in the power section.

```
Node and link data:
-------------------------------
 0    Gnd
 1    Pwr
 2    Link       19 29
 66    Meas only
```

  The first column is the node number. Another column displays other nodes that are connected to this node.

- **Leak Data**

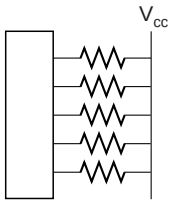
  Leak data (parallel and series) describes a leakage path which is below the minimum impedance necessary to qualify as a parallel path for a DeltaScan test (default 10k ohms). Each group of nodes is connected by some impedance. Two pins from this group cannot therefore be used to create a valid pin-pair.

  Leak data looks similar to the link data displayed above, but conveys different information: the data concerning the leakage of current between nodes on the board. To derive this data, DeltaScan reduces each component to an equivalent impedance. For speed, there are several approximations made in this analysis, which always errs on the conservative side. Resistances between nodes are assigned ranges. For example, in the sample report below, 100R-1K means that node 24 has between 100Ω and 1kΩ of resistance to other nodes listed in that row.

```
Leakage path data:
-------------------------------
 0    1K-20K    12 82
 1    Link        18
 5    Link        10
 6    Link         25 11 13
14    1K-20K     16
22    100R-1K    21
24    10-50R      38 336 328 35 34 23 42 337
```

Troubleshooting Leak Data If the leak data shows an extremely large number of leakage paths, it often indicates that power and/or ground nodes have not been conveyed correctly. This is because impedances to ground or power that are above a threshold are discarded since they do not affect tests. If the power or ground is missing, then they become leakage elements.

For example, consider the bus with pull-up resistors shown here. If the power is not correctly identified, then all of the pins on this bus will leak to each other and they cannot therefore be tested (if the pull-up resistance is high enough). Whereas if the power was identified correctly, then they are all testable.



Assuming each R>100Ω

Board Layout Considerations

The following characteristics of a circuit board will have an affect on DeltaScan measurements.

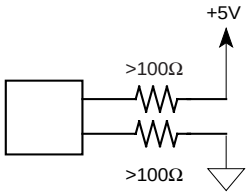
Unique Pin

DeltaScan requires a unique signal path so it can verify the substrate path through a device. If all pins on a device are connected to another device, the first device is not testable. However, if even one pin on the first device is not connected to the other device, the device is testable because of that unique pin. If a pin is lifted on the first device, we still get a good signal from the other device.

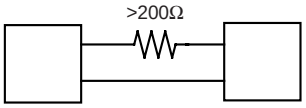
A unique signal path is not generally a problem with large ASICS on a board, but can be a problem testing memory devices where most or all pins connect to one device. A unique signal path can also be a problem where banks of memory are placed in parallel, except for one or two pins. In this case, a smaller signal will often result due to the reduced number of test-path possibilities.

Pins Connected to One Device or Banks Of Memory Placed in Parallel

For devices that have pins connected to one device or banks of memory placed in parallel, it may help to make sure the unused pins have tester access and are not tied to the power rails. If a pin must be biased to either power rail, you can use a pull-up/ pull-down resistor, greater than 100 ohms.



Pins with No Unique Path Where no unique path can be guaranteed, a series resistor 200 ohms or greater placed in a non-critical signal path can achieve the required unique pin. See also “Bussed Pin Groups” later in this section.

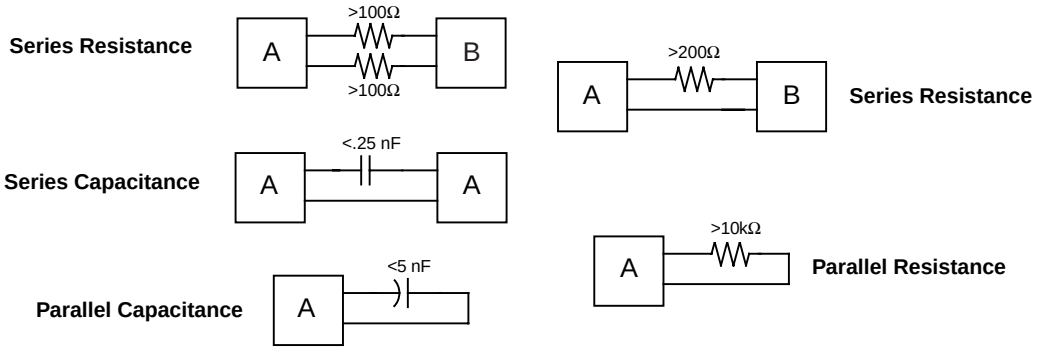


Discrete Components

A DeltaScan test works well in the presence of discrete components. The limits are approximately:

- Parallel resistance between pins on a device > 100KΩ
- Pull-up/down resistance > 100Ω
- Series resistance to other components > 200Ω
- Series capacitance < 2.5µF
- Parallel capacitance < 5nF

The above values use this formula to calculate capacitive impedance: 1µF ≈ 50Ω; capacitor resistance is derived from 1µF*r ≈ 50/r.



Tied Pins

Where two or more pins on the same device are connected together via the printed circuit board (PCB) traces, it is not possible to detect an open circuit unless all the tied pins are open. For this reason, tied pins are considered not covered for opens and count as missed faults in the coverage figures.

Bused Pin Groups

Frequently, buses are allocated to a contiguous group of pins inside an IC. DeltaScan relies on measuring the common substrate resistance between two pins. This signal is reduced when the pins are separated by a ground connection and is often not measurable when they are separated by two or more ground connections.

Signal reduction is aggravated by the common practice of including a ground connection at each end of a bus inside the IC. As the pins within a bus often provide no possibilities for a unique test path, it is necessary to go “across the ground” for the second test pin. The result is that the pins can have insufficient signal even when there appears to be a path.

Noise

A circuit board incorporating a ground plane poses no problem. However, you must take precautions to prevent unwanted signals from being generated across the board trace resistance of a board without a ground plane. If it is not possible to maintain good ground integrity, the measurement achieved may report false passes and/or false fails.

To maintain the optimum ground reference, DeltaScan can sense the ground at each component if necessary. To do so, you need to wire a reference node near the specific device and enter this special reference node in the worksheet for that device, using the local reference.

Refer to “MultiScan Reference Node” on page 1-16 for information.

DUT Power Supplies

During the DeltaScan test, it is necessary to connect the board power supply traces to ground to prevent stray leakage paths via the supply rail and ensure that the signal being measured comes only from the device being tested. Failure to connect the power traces to ground results in tests that appear to verify pin pairs that will pass when the pins are actually open.

If the board has components connected to board-generated supplies or on-board regulators, for example, you must ground these supplies as well as shorting the input power supply for the duration of the DeltaScan test.

The board supplies do not have to be shorted when a device is powered by a unique supply such as a single battery backed RAM. Higher signal levels with consequently higher fault coverage may be obtained if the supplies are not grounded.

Unconnected Pins

If there are many unconnected pins, it may prove beneficial to nail some, but not all of them. “Unconnected” refers to pins that are not used in the board, but are actual input or output on the device. Unconnected pins are referred to as “N/C” in the DeltaScan editor. Unconnected pins often have no test nails assigned when the test fixture is built, despite the fact that these pins have a device function. A short circuit on these pins affects circuit operation in different ways and may shorten component life (if the unconnected pin is an output).

If a test nail is fitted, there are two advantages: the pin can be tested for short circuits, and it can be used for DeltaScan tests. By virtue of its lack of board connection, it offers a unique test path and is often preferable to using connected pins.

Multipanel Boards

Wiring for multipanel boards requires special attention:

- Each board panel should have a unique reference node for sensing its ground plane.
- If the number of power rails exceeds the number of DeltaScan shorting pins available on the DeltaScan board, use the Relay Array Board or fixture relays.

Onboard Batteries

Many computer motherboards are now fitted with batteries during the ICT process. This causes no problems for the DeltaScan test, but may cause undesirable stress on the battery because the DeltaScan technique involves forcing all power and ground rails to DeltaScan analog ground.

Mark the nodes connected to the battery as no-connect (9999) on the device worksheets and on the Component Properties section of the power tests so that the DeltaScan system will not drive them.

DeltaScan Fixturing Requirements

Additional fixture wiring must be added for DeltaScan testing. This wiring establishes solid grounding relative to DeltaScan's ground. Grounding prevents stray currents from producing a false delta measurement.

DeltaScan Relay Wires

Each DeltaScan relay wire connects one DeltaScan relay to one fixture pin on each power or ground rail. These relays sink all the current produced by the DeltaScan stimulus and measure sources and prevent the voltage that could affect Delta from developing.

- **To add power and ground buses:**

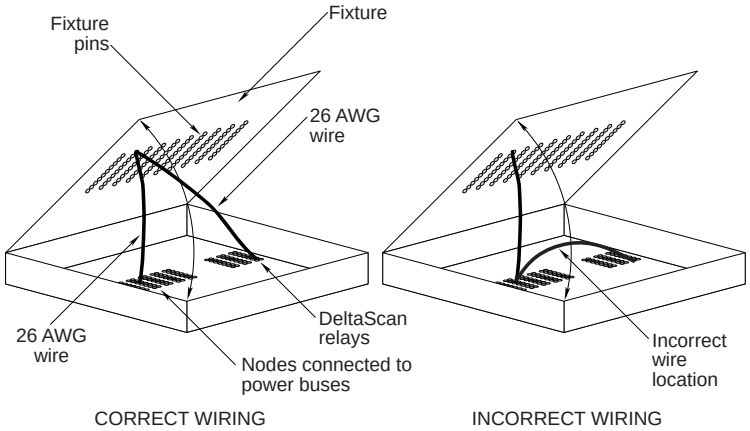
1. Identify the power buses on the board, and record all power and ground bus nodes for later use during program generation.

   Power buses include:

   - Power/ground from off-board connectors
   - Power/ground from on-board regulators
   - Power/ground from in-line inductors

2. Wire each power and ground bus fixture pin to a DeltaScan Relay node in addition to its currently assigned node.

   These DS Relay nodes are near the DUT power and ground nodes on the right side of your fixture receiver.



3. If you have more power and ground buses than the eight DS Relays, wire ground, then the most commonly used supplies, until all eight DS Relays are used. Then use G-Pole shorting for the rest.

   All current flows through these relays to the DeltaScan ground. This grounding is required to ensure that stability and signal levels are correct.

   For more information, see **Z1800-Series Fixturing Guidebook**.

G-Pole Shorting

G-pole shorting is a new feature with F.2a system software. If you have more than eight power and/or ground buses, you will not have enough DS Relays during fixturing. You will need to turn On the PRGMVARS /DeltaScan/ Short Pwr/Gnd via G-Pole. This selection will connect all power and ground nodes found in power worksheets together through the G-Pole during DSCAN testing, thus connecting all remaining power buses to the DS Relays. It is critical to have accurate power information and to have used all the DS Relays first so that G-pole shorting can work correctly.

Note: DSCAN cannot use G-Pole shorting on nodes in the same 16 node group as the reference node. Such power/grounds must have a DSCAN relay wire.

Device types recognized by DeltaScan:	IPL Tokens
Adjustable PS A	PWRA
Adjustable PS B	PWRB
Fixed/Slave PS A	PWRA_F
Fixed/Slave PS B	PWRB_F
PB	PB
Power 5.5V	PWR5_5
Power 5V	PWR5
Power Bus	PBUS

Power Steps with More Than Two Pins DeltaScan assumes that the first pin of a power step is the power rail and the second pin is the ground rail. Pins 3 and higher are ignored for all power steps, but DeltaScan needs to know about the nodes assigned to these pins. Therefore, if you have power steps with more than two pins, put the nodes from pins 3 and up into new, disabled PB steps in the pin 1 and 2 positions.

If you generate these power steps from an IPL, rather than manually creating these power steps, include all relevant nodes so that the Component Properties will be correctly filled in. (Node entries in the Test Properties part of any worksheet are considered test data, not topology data, and are ignored.)

MultiScan Reference Node

The MultiScan Reference node wire connects an unused node to a new fixture pin which contacts the ground trace of the board under test when vacuum (or other pull-down mechanism) is applied. Establish a Multiscan Reference node if one does not already exist. This node allows DeltaScan to sense the voltage level of ground on the board under test. No current should flow through this path if it has been set up correctly.

The global reference node is stored in the Header/PRGMVARS step in the MultiScan Reference Node field. It should appear in the MultiScan Reference Node field, not in the list of Ground Reference Nodes. The reference node default is 9999.

The reference node default in the PGEN.CFG file is also 9999. You can specify the reference node by editing Header/PRGMVARS or PGEN.CFG file, as explained in “Update PGEN.CFG” on page 1-20.

If you want to use a reference node that applies only to one test, set a local reference node in the Test Properties section of the worksheet. See “Test Properties Fields” on page 1-27.

Selecting a Reference Node

The reference node should be different from any of the ground node(s) which are wired to the chips to be tested. It should connect only to the ground node(s) through board traces when board vacuum and fixture vacuum are both On.

Remember, the reference node can be any available node, but it will be used as a high impedance sense path (Kelvin connection) to the DUT ground. This means that (ideally) NO CURRENT will flow through this wire during testing.

The selected reference node must be the same node as is wired in the fixture. Although you can use any valid unused tester node number as the reference node, it is recommended that reference nodes be chosen from available Sense nodes. If the program uses the G-pole for power-supply grounding, the reference nodes must be chosen from available Sense nodes.

The reference node should not be tied to the same nail that connects the board ground to the DeltaScan pins, or to the system power supply grounds. It should have only one wire: the reference node wire.

The reference node must be in a different 16-node group from the device ground and from any power supply. For example, if you have a device ground at node 0, put the MultiScan Reference at node 16. Do not use the system ground node 0 as the reference node. Use node 16 when possible.

Checking Reference Node Wiring

Wiring errors in the reference node cause currents to flow in the reference path, resulting in erroneous readings. Teradyne recommends that you choose an available sense node from the fixture interface. This means that the node is in the upper 16 node group of the D/R board. Any power supplies connected to the same 16 node group on any D/R board cannot use G-Pole shorting for grounding.

The fixture probe that contacts the board ground trace should have only a single wire on it. The wire connects the DUT board ground to a node in the tester. A common error in wiring the reference node is the addition of wires to the fixture ground plane, V reeds, or DUT power supply. Record the reference node you have established for later use during program generation. This reference senses ground at the board under test. Establishing the proper reference node is mandatory for dependable DeltaScan results.

You can verify that your reference node is wired correctly by removing the board and pressing Start (with the fixture still pulled down).

- **To verify reference node wiring:**

  1. Wire the ground reference to a nail contacting the board ground trace.

     This nail should have no other wires attached to it.

  2. Remove the test board.

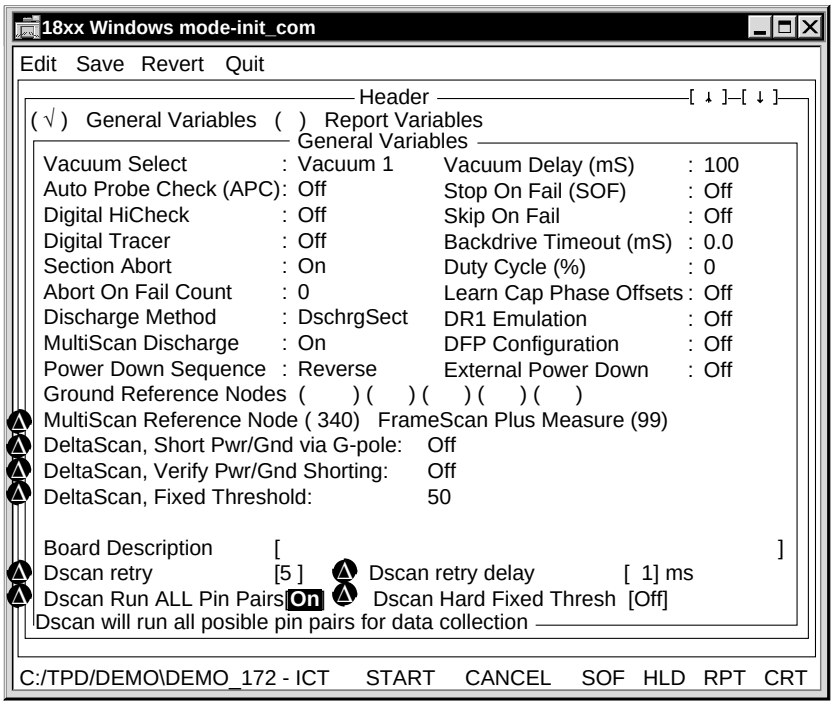
  3. Select **Start** and verify that the system gives an error message.

     You should see a message saying that the reference node was NOT detected. If you do not, your fixture is miswired. This procedure will not find every possible reference node problem, but it is very effective.

DeltaScan PRGMVARS

Header/PRGMVARS includes the following General and Report Variables variables specific to DeltaScan testing. If you use DeltaScan, know what these variables do and set them as needed.

For a description of all fields in Header/PRGMVARS, refer to the **Z1800-Series Programmer's Guidebook**.



DeltaScan variables

General Variables

- **MultiScan Reference Node**

  Senses the actual ground level of the board under test. This global reference node can be overridden by local reference nodes defined in individual test worksheets. The default is that each component test uses the global reference node defined in PGMVARS.

Note: The default MultiScan reference node in the PGEN.CFG file is 9999. You can specify the reference node by editing the PGEN.CFG file before generation or entering the reference node in Header/PRGMVARS at any time.

- **DeltaScan, Short Pwr/Gnd via G-pole**

  Enables DeltaScan to use the G-pole for power and ground nodes if there are more than eight (the number on the DeltaScan board); the default setting is On.

- **DeltaScan, Verify Pwr/Gnd Shorting**

  When G-pole shorting is Off, verifies that all power and ground buses have proper grounding; default is Off.

- **DeltaScan, Fixed Threshold**

  Fixed test threshold value used by all DeltaScan tests that specify a fixed threshold.

- **Dscan Retry**

  Number of times DeltaScan should retry testing a particular pin-pair before marking the test as a failure and going to the next pin-pair. If a pin-pair passes during any of the retries,it passes and is not retried again. The pin-pair must fail all of the retry attempts to be a failure. This feature is useful for pin-pairs which are not stable.

- **Dscan Retry Delay**

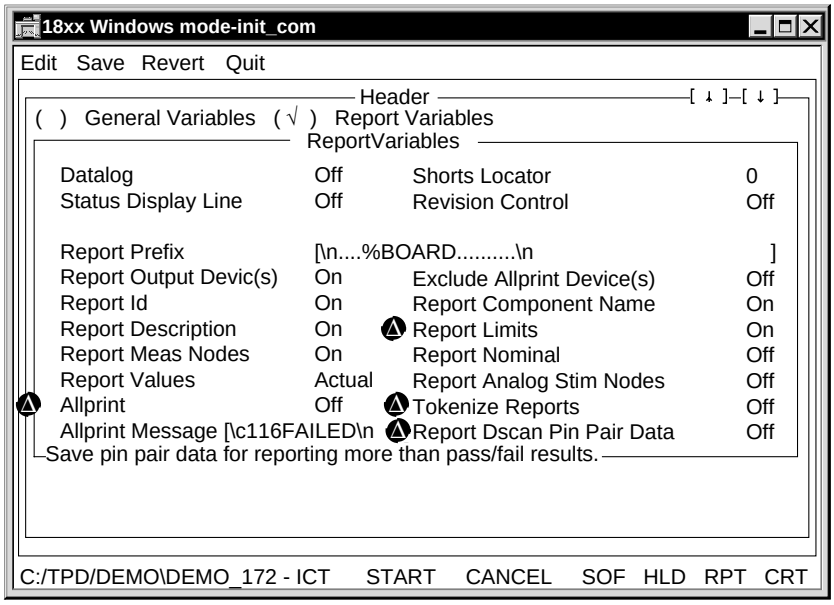
  Number of milliseconds to pause between each retry.

- **Dscan Run All Pin Pairs**

  Executes all possible pin pairs regardless of whether pin pairs pass or fail. Normally DeltaScan runs only enough of the pin pairs in the DSCAN.DB database necessary to pass each pin. Using this feature increases the amount of output data for both Datalog with Allprint selected, and Tokenlog. This feature is useful for collecting data on all possible pin pairs for stability analysis.

- **Dscan Hard Fixed Thresh**

  DeltaScan tests use the fixed threshold for all pins, rather than the lower of the fixed threshold and one-third of the learned value.



DeltaScan variables

Report Variables

- **Report Dscan Pin Pair Data**

  Off: DeltaScan pin pair data is not sent to the diagnostic channels.

  On and Allprint is Off: Only pin pair data for failing pins is sent to the diagnostic channels.

  On and Allprint is On: Pin pair data for all DeltaScan pins is sent to the diagnostic channels.

Note: This can reduce throughput, especially if “run all pin pairs” is active.

- **Allprint**

  On: A report is generated for every test, not just the failing tests.

- **Report Limits**

  On: The report includes the Pass/Fail limits of the test.

- **Tokenize Reports**

  On: Datalog and CRT reports are in Tokenlog format. The report file is TOKENLOG.DAT and is in the TPD\PROGRAM directory.

Developing DeltaScan Tests

To achieve maximum coverage without false passes, false fails, or unstable tests, complete topology is required. All components and interconnect data should be represented in your program before you start, except, of course, for components which will be tested by DeltaScan.

Jumpers, continuities, capacitors, inductors, resistors, and non-DeltaScan digital components must be entered in your program before you validate your DeltaScan tests, to prevent creating tests with false passes or false fails. The interconnect steps should be complete and functional.

The other steps (both analog and digital) need only to have their Component Properties correctly filled in (nodes, values, and IDs).

Note: It is best to add DeltaScan tests after you have entered all other topology information and have run Learn Interconnects.

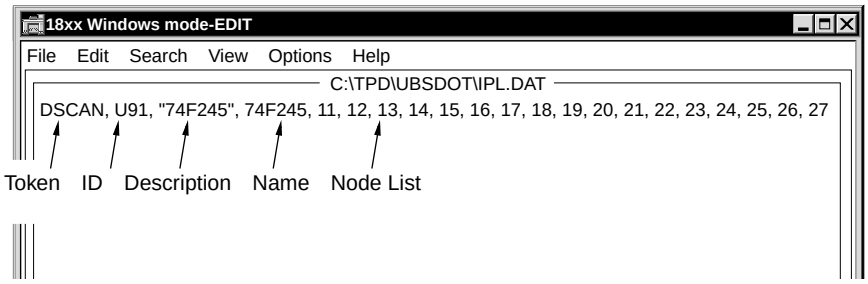
- **To develop DeltaScan tests:**

  1. Set up DSCAN tokens.
  2. Build the necessary database files.
  3. Generate the test.
  4. Validate and troubleshoot the test.

These steps apply, in some form, whether you are adding DeltaScan to an existing board test or developing tests for a new board. The differences are discussed in each step.

Set Up DSCAN Tokens

The input list (IPL) is an ASCII file that contains a complete description of the board component parts and interconnections. For each DeltaScan test, modify the IPL syntax by adding an IPL record to support the DeltaScan test type.



IPL Record

A record is a section of the input list file IPL.DAT dedicated to a single component test step. Like all other component tests, a DeltaScan test is governed by its input list record.

Refer to the **Z1800-Series Programmer's Guidebook**, Chapter 7, "Program Generator Tools," for more information about record syntax in general.

- **To add a DeltaScan test to a new board test program:**

  Start from the input list. Modify it by adding an input list record to support the DeltaScan test type.

- **To add a DeltaScan test to an existing board test program:**

  1. Rename the original IPL file, giving it a different extension.

     This preserves the original IPL while you create an incremental IPL.

  2. Create a new IPL.DAT and add DSCAN entries.

     Digital entries from the original IPL can be copied and converted to DSCAN entries.

     If you are adding DSCAN tests for WSCAN components, you will need to remove the inducer number from the newly formed DSCAN entries. Ensure that you don't create more than one DSCAN test for the same physical component or your coverage on all tests for that component will go to zero with all pin types set to NO PATH.

Major and Minor ID DeltaScan topology relies on the concept of major and minor IDs.

- The major ID is the part of the ID that comes before a dash or hyphen (-) or an underscore (_).
- The minor ID is any part after the major ID, including the dash or underscore.

In U1_A, for example, U1 is the major ID and _A is the minor ID.

Follow the Major/Minor ID convention for all components. This especially applies to devices tested with both DeltaScan and other tests methods. (example U1_dscan, U1_vec) These connections determine which pin pairs will be included or excluded from the final tests based on impedances to each other and to power or ground.

Add a unique minor device ID to each new component entry. For example, use _DS, so that U37 becomes U37_DS. The major device ID, U37, will not be in conflict with U37_DS.

Set Up Power Information

For DeltaScan tests, you must specify all power and ground buses. Power buses include the output of on board regulators and any device power pins that have connections through inductors.

Often the only power steps identified in a test program are those where the Z1800 power supplies are controlled. In addition, there may be:

- Board-generated supplies
- Voltage regulators
- Additional buses connecting to 18XX power supplies via inductors

If integrated circuits tested with DeltaScan have power pins that connect to such power nets, the nodes of the power nets must be included in the program by using a PB token in the IPL.DAT before generation or by adding a power-bus step in the power section and updating. Even if your program is an analog-only power-off program, you still need these power statements, but you also need to disable the final power steps.

Note: Missing or incorrect data for power and/or ground buses can cause Validate to take more than ten times longer to complete and will probably result in drastically reduced coverage.

- **To set up power information for a new board test:**

  1. Add entries to IPL for each power bus identified. This automatically ensures that the relevant nodes are entered in the Component Properties sections of the worksheets.

  2. If you do not want to execute these steps, disable them after generation. DeltaScan is still able to use the topology information from the disabled steps.

- **To set up power information for an existing board test:**

  1. Make sure that all identified power buses are in the program. If not, add them to the incremental IPL along with the DSCAN tokens.
  2. If the incremental generation is partial, or if you did not need to do it at all, examine the existing power steps to verify that the power nodes are recorded in Component Properties/Number of Pins/Node Entry and that the reference nodes are all in Pin 2 of the Component Properties/Node Entry.

Note: Custom nodes used in the Test Properties section of the worksheet are not seen by DeltaScan.

Update PGEN.CFG

Settings in the PGEN.CFG file configure the program generate function. You can edit the PGEN.CFG file to specify other DeltaScan test default values for PGEN instead of the standard defaults. For a complete discussion on editing the PGEN.CFG file, refer to the **Z1800-Series Programmer's Guidebook** Chapter 7, "Program Generator Tools."

Note: Several DeltaScan variables that are set in Header/PGMVARS are also set in the PGEN.CFG. When you generate the tests, PGEC.CFG writes these variable values back to PGMVARS:

- MSCANREF, MultiScan reference node.
- MAJRSEP, characters used to separate the major and minor IDs.
- DSFIXTHRESH, the fixed threshold value of new DeltaScan tests.

The following fields in the PGEN.CFG file apply to DeltaScan:

- **DISABLEPWR**

  Defining power leads is required for a DeltaScan test, but defining the leads normally causes generation of a power test.

  Disable power causes the automatic generation of disabled power tests when power nodes are defined.

  The DISABLEPWR default is No. If you don't want to execute any power tests, set DISABLEPWR to Yes.

- **MSCANREF**

  MultiScan Reference node is an otherwise unused node that specifies the reference node for a DeltaScan test. The MultiScan Reference node is stored in the Header/PRGMVARS worksheet of the test program for the board.

  Although the default is 9999, the value should be set to a valid reference node. You can specify the reference node by editing the PGEN.CFG file before generation or entering the reference node in Header/PRGMVARS at any time.

  PGEN adds this node to the Header/PRGMVARS Multiscan Reference node field during incremental program generation.

- **MAJRSEP**

  The characters used to separate the major and minor IDs in component IDs. Up to four characters can be designated as separators; the default separators are the underscore and the hyphen.

- **DSDEFTHRESH**

  Designates the default DeltaScan test threshold: Low, Nominal, High, or Fixed.

- **DSFIXPIN**

  The maximum number of device pins a device can have and still be assigned the fixed threshold type. The default is 32.

- **DSFIXTHRESH**

  Determines the fixed threshold value for newly generated DeltaScan tests that have no more than the maximum number of pins set in DSFIXPIN. The default value is 50.

  PGEN adds this value to the Header/PRGMVARS DeltaScan, Fixed Threshold field during incremental program generation.

Build the Database File

Once edits are completed, save the IPL, and continue with these steps:

- **To build a new board test:**

  1. Run **PGEN/CLEAN**.
  2. Run **PGEN/BUILD**.

     This command creates a new temporary IPL database, IPL.DBF.

- **To build an existing board test:**

  Do NOT run PGEN/CLEAN. Run **PGEN/BUILD**.

  If you accidentally select PGEN/CLEAN, copy the board directory from your backup and start over.

Learn Interconnects

The PGEN/LEARN command finds continuities, special cases, shorts, and merged special cases. For details on learning interconnects, see Chapter 7, “Program Generator Tools.” in the **Z1800-Series Programmer’s Guidebook.**

If any of the device nodes are connected to other nodes via low impedance paths and have not been added to the appropriate interconnect group, you should add these nodes to the appropriate interconnect group now.

- **Learn interconnects for a new board test:**

  Run **PGEN/LEARN**. The system inserts the interconnect test steps into the program.

- **Learn interconnects for an existing board test:**

  Assume that PGEN/LEARN has already been run. If in doubt or if topology has changed at all, run it again.

Generate a Test

The PGEN/GENERATE command automatically generates the test program ICT.TST from the IPL. The process for developing and executing a test program that uses DeltaScan is the same as the existing processes for developing a Z1800-Series test program.

The three test generation methods are automatic program generation, incremental program generation, and manual program generation. They are described in the **Z1800-Series Board Test Tutorial**.

Important: The Programmer Efficiency Package (PEP) does not recognize DeltaScan tokens and will not perform an analysis on them in the input list.

- **To automatically generate a test:**

  1. Run **PGEN/GENERATE**.

     This command adds the IPL.DBF entries to the main test program ICT.TST. Do not be concerned about messages regarding missing power or ground. Updating and subsequently running Validate eliminates such messages.

     A DeltaScan test can only be generated once from the DeltaScan worksheet. If regeneration is required later, the original device must be deleted.

2. Run **PGEN/UPDATE**.

   This command is needed to finalize topology for all reports and before any Validates. The update is critical for success.

3. After generating DeltaScan tests, review the resulting worksheets.

   Make sure that the Multi-Scan reference node, thresholds, nodes, etc. have been set correctly:

   Your EXCEPT.LST will probably note that power/ground pins are missing. Such messages are normal for DeltaScan incremental generation. This problem is resolved during Validate.

Validating and Troubleshooting Tests

Use PGEN/VALIDATE and your own analysis of system worksheets and reports to achieve maximum test coverage and eliminate false passes, false fails, and unstable tests.

The Validate process puts test steps through an automatic analysis process. In addition, the DeltaScan worksheets, Topology and Board Fault Coverage reports, and DeltaScan database all provide information for troubleshooting tests.

Make edits to the worksheets and the database, as needed, to improve the tests. Follow this process:

- First, look at the Topology report for component node and ID problems. Edit the test program ICT.TST before you run Validate. Recheck the Topology report.
- Validate the tests.
- Look at the DeltaScan worksheets, Board Fault Coverage report and the DeltaScan database file. Modify or add pin-pairs, threshold values, etc. in the database or worksheets.
- Continue to run Validate and edit component and test attributes until you have the program perfected.

This section covers validating and troubleshooting suggestions, tools and processes. For complete information, also read Chapter 7, “Program Generator Tools” and Chapter 9, “Test and Debug Tools” in the **Z1800-Series Programmer’s Guidebook**.

Analyze the Topology Report

Select PGEN/Reports and generate the Topology report. This step is critical in the process for good fault coverage. Study the report after reading the “Managing Topology” section of the **Z1800-Series Programmer’s Guidebook** about sharing component IDs and nodes.

Edit the test program ICT.TST to correct any problems you uncover.

Component Node and ID Problems

TOPOLOGY.LST, the Topology report, lists component groups that share identical IDs but different nodes. Make sure that the IDs correctly show the number (one or more than one) of physical components; the same component should have the same major ID at each mention.

The Topology report also lists components that specify the same nodes but have different IDs. In those cases, make sure that different physical components have different major IDs.

Parallel jumpers, and other low-resistance components with at least **one** common node appear in TOPOLOGY.LST as having matching nodes. This is because all nodes are electrically connected and therefore appear identical to the report software. No action is needed in this case.

Two problems, along with likely causes and solutions, are detailed below.

Zero Coverage and No Path Status Sometimes a component may show zero test coverage, with “no path” status on its pins. A possible cause is the component record listing the same nodes as a component with a different ID. If the two records are for two truly different components with identical nodes, DeltaScan testing is not appropriate. However, if the two records actually represent the same component, the major IDs should be made identical (though the minor IDs should be different).

For example, a single 68020 device on a board might be listed in two records as follows:

```
DSCAN, U1A, "Micro", 68020,6,17, 34
VEC, U1B, "Micro", 68020,6,17, 34
```

This condition will be reported in TOPOLOGY.LST under “Reporting - components with different IDs but matching nodes,” as shown below.

```
# Reporting - components with different Id's but matching nodes. #
=======================================================
 Check group -
Id ='U1A'Section = DeltaScan Token = DSCAN
Id ='UIB'Section = Digital Token = VEC
```

The solution would be to adjust the two different IDs in the worksheet, so that they appear with the same major ID and different minor IDs:

```
DSCAN, U1_A, "Micro", 68020,6,17, 34
VEC, U1_B, "Micro", 68020,6,17, 34
```

Tied Pins Not Appearing in DeltaScan Worksheet Some components to be tested with DeltaScan may have tied pins that will not appear with “Tied” status in the worksheet.

The cause may be that the records for surrounding components have the same major ID but different nodes; during Validate, complete topology data will not be created for DeltaScan. The solution is to make the IDs different.

For example, two records might appear as follows:

```
L, L701A, "PEB53741", 10H,20.00%,106, 146
J, L701A, "PEB53741", 106&150
```

The condition will be reported in TOPOLOGY.LST under “Reporting - components with matching IDs but different nodes.”

The solution would be to make the identical IDs unique in the worksheet, perhaps by changing the second L701A to J701A:

```
L, L701A, "PEB53741", 10H,20.00%,106, 146
J, J701A, "PEB53741", 106&150
```

This indicates that two low-impedance components are involved, not just one.

Validate Tests

The Validate function attempts to improve DeltaScan tests by using various combinations of stimulus, measure, and guard configurations, wire modes, and wait times while testing known good components.

This process is the same whether you are developing a new board test or adding DeltaScan components to an existing board test.

If you are adding a few DeltaScan components to existing DeltaScan tests, revalidate and troubleshoot the whole section since the topology has changed.

- **To validate the test program:**

1. Select **Validate** from the Setup menu.

   The system displays the Validate Configuration window.

2. Select **Validate DeltaScan**.

3. Set the following **DeltaScan parameters**:

   Important: Start with the defaults for these values unless you are in the troubleshooting phase.

   - Minimum Parallel Resistance: Pins with less resistance than this value are considered No Path. Default 10. Range 1–20 kOhms.
   - Minimum Series Resistance: Series resistance (chip to chip and back) lower than this value results in No Path. Default 200. Range 50–1000 kOhms
   - Nominal (100%) Learn Threshold: Pin pairs with a Delta measurement below this value are not used. Default 150. Range 0–2000
   - Threshold for first measure of a Delta: Default 1024. Range 1–2000
   - If Threshold exceeded: Warn/Disable.

4. Check the **Discharge settings in PRGMVARS**.

   DeltaScan uses the Discharge method/discharge section if the PRGMVARS MultiScan Discharge is On, regardless of the setting of Discharge Method. Therefore, make sure that the section is complete, correct, and enabled.

   Tests in your Dscan section that fail in Run mode but pass when started from the worksheet are indication that you need to run the discharge section.

   Note: Turning off Discharge may be dangerous. Capacitors can build a charge from any previous component or board run. DeltaScan connects all power and ground nodes to its own analog ground. This could short out charged capacitors.

5. Run **Validate** from the DeltaScan section or DeltaScan component editor.

   At this point, using a known good board on the fixture, run Validate from the section menu or DeltaScan editor to produce workable test parameters for that particular device on that particular board. (Before initial validation, tests all have 0% coverage and will pass if executed.)

   It is assumed that known good boards are used for validation. If you are not sure of the quality of the available supply of boards used for Validate, you need to examine each DeltaScan test, determine the cause of coverage problems, correct them if possible, then re-validate.

   Note: Do not run Validate until every component has a component ID with correct node numbers, or results might not be dependable.

Validate can either Learn New Data or Add to Existing Data, and Keep Disables (meaning to keep edits that disabled pins or device) or Enable All.

The available thresholds are 200%, 100%, 50%, or 30%, with DeltaScan unit equivalents as listed below.

100% = 150 DeltaScan units
200% = 300 DeltaScan units
50% = 75 DeltaScan units
30% = 45 DeltaScan units

It is valuable to try Validate with a higher threshold on specific intermittent tests. In some cases, it is necessary to re-run Validate.

6 Troubleshoot any failures.

If you are using F.2 (or later), turn on Edit/Header/PRGMVARS/General/DSCAN Hard Fixed Thresh. Retest the DeltaScan section with SOF on and disable any failing pin pairs. Then turn DSCAN Hard Fixed Thresh off.

A useful technique for eliminating unstable tests:

- Edit your first DeltaScan step and click the upper left button in Test Properties to get into the DeltaScan editor.
- Turn on SOF and RPT.
- Press Start and fix any problems by disabling failing pins.
- When you can let the step run without failing for at least thirty seconds, save the step and go to the next step.

For more troubleshooting techniques, see the following sections.

7 Run **Validate** on additional boards.

Use the Validate feature “Add To Existing” against additional boards to build a database that will be stable across different boards.

8 Revalidate individual devices as necessary to get repeatable and stable tests on the sample boards. Use Add to Existing for different device manufacturers.

Revalidation will build a database that will work for multiple vendors. In some cases, intermittent failing pins may need to be disabled. In other cases you may be able to solve problems by deleting pin pairs after clicking on the pass or fail for a given pin in the DeltaScan editor.

9 Make sure all pins shown as power and ground in the schematic have power and ground status in the worksheet and all pins shown as tied in the schematic have tied status in the worksheet.

MultiScan Failure Flag A system flag called MultiScan Failure is set if any MultiScan test, including DeltaScan, fails. If the Section Abort feature is enabled, a failure causes the software to jump to the Trailer.

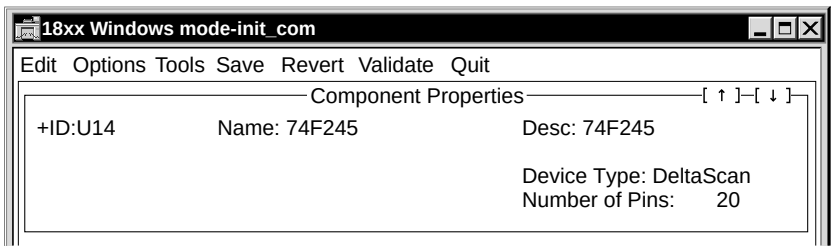
Troubleshoot Tests

This section contains suggestions for making test program corrections. Start troubleshooting by examining the test worksheets and reports.

Edit the DeltaScan Worksheets

Use the fields and controls of the DeltaScan worksheets to troubleshoot tests.

Component Identifier Section The Component Identifier section of a DeltaScan worksheet specifies the information required to generate a DeltaScan test for a component. You previously set up the information by running Build and Generate on the IPL or manually adding a DeltaScan component and filling in the information on the worksheet.



Component Identifier Fields

- **ID**

  Component identifier. For example, “U14.” The + preceding the ID indicates that the step is enabled.
- **Name**

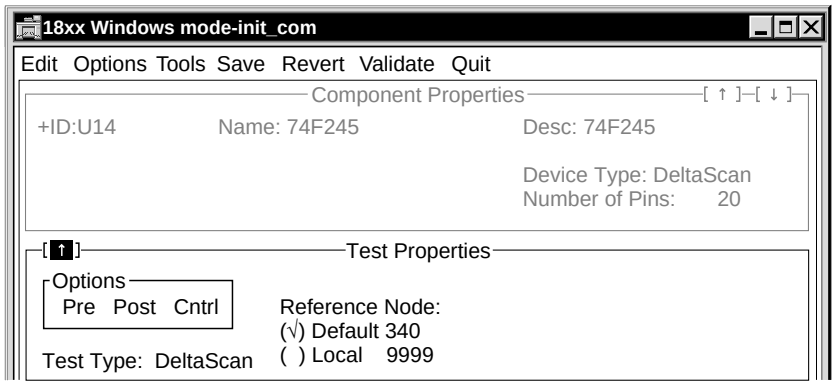
  Device name.
- **Desc**

  Text description of the test. For example, “IC Pin Test.”
- **Device Type**

  DeltaScan
- **Number of Pins**

  Total number of pins on the component.

Test Properties Section The Test Properties section of a DeltaScan worksheet displays test parameters and results. From here you edit and execute the test step.



Test Properties Fields

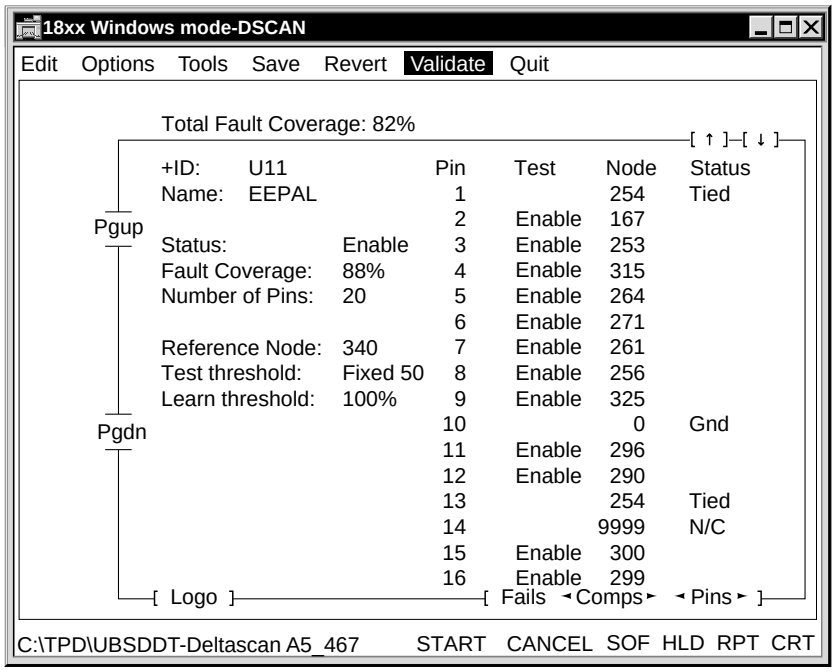
- **Arrow**

  Displays the DeltaScan editor and the test data described below.
- **Options**

  Displays the Pre-Test, Post-Test, and Test Page Control options.
- **Test Type**

  DeltaScan.
- **Reference Node**

  MultiScan Reference node number, global (from PGMVARS) or local.



Test Data Fields

- **Total Fault Coverage**

  Coverage for the entire board under test.
- **ID**

  ID of the current component. Field can be edited. Entering a new component ID displays information for that component.
- **Status**

  Shows whether this device is enabled or disabled for DeltaScan testing.
- **Fault Coverage**

  Actual fault coverage for this device.
- **Number of Pins**

  Number of pins on the device.
- **Reference Node**

  Reference node number for the device under test. The node can be a local reference node for this particular test or the global reference node defined in the PGEN.CFG file MSCANREF field.

- **Test Threshold**

  Changing to different threshold levels can help identify unstable tests.

  - High, one-half the threshold determined by Validate
  - Low, one-fourth of that determined by Validate
  - Nominal, one-third of that determined by Validate
  - Fixed threshold of 50.

- **Learn Threshold**

  Minimum change in current considered sufficient for a valid test; the choices are 200%, 100%, 50%, and 30% of the threshold determined during Validate.

  Threshold equivalents in DeltaScan units:
  100% = 150 DeltaScan units
  200% = 300 DeltaScan units
  50% = 75 DeltaScan units
  30% = 45 DeltaScan units

  Make judgments on the quality of the tests performed on the device by looking at the Stim Pin/Learn Data for the device. The magnitude of the Learn Data is one indication. The Learn Data is the actual value measured during validation.

  Validate uses the learn threshold to determine if a pin pair produces enough signal for a valid test. When the learn threshold in the worksheet is set at 100%, a measured value of 150 is the minimum that Validate accepts.

- **Pin**

  Pin number.

- **Test**

  Click to enable or disable all tests for a pin.

- **Node**

  Node number.

- **Status**

  Shows the reason for not testing pins that DeltaScan doesn't test.

  - N/C–Not Connected
  - Power–Power and ground leads for the device
  - No Signal–Insufficient signal for level set by Validate learn threshold for test produced by any possible pin pair.
  - No Path–No other pin on the current device does not connect to this pin.
  - Tied–Pin is tied to another pin on the current device.
  - Unstable–No stable (repeatable) test reading obtained.

Note: When a DeltaScan test runs, the Status column shows Pass or Fail, depending on the results of the test. Clicking on Pass or Fail displays the tests that ran for the pin. You can delete pin pairs and edit thresholds.

- **Next Component, Prev Component**

  The vertical arrows above the Status field display the previous (up) or next (down) component when clicked.

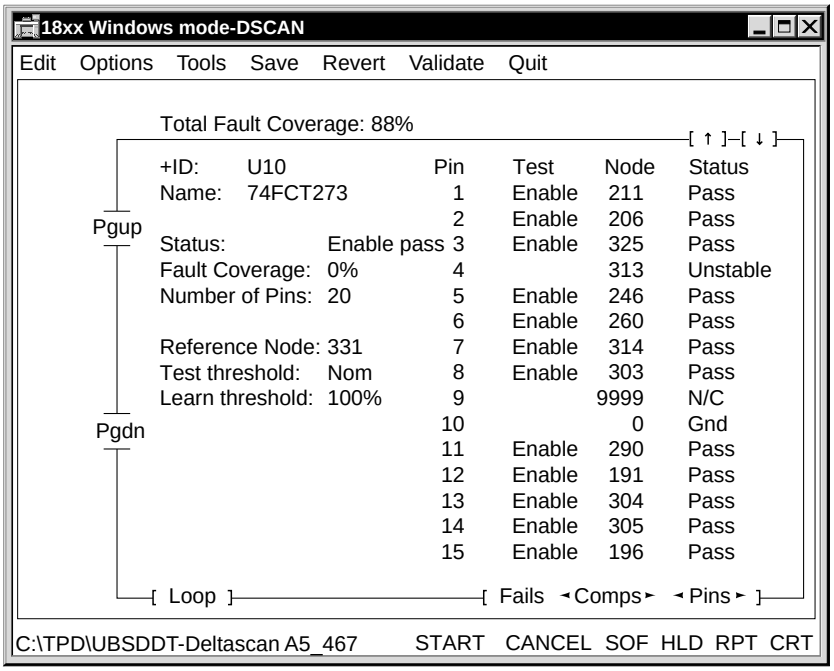
- **Loop**

  Click to repeat a pin-pair measurement continuously.

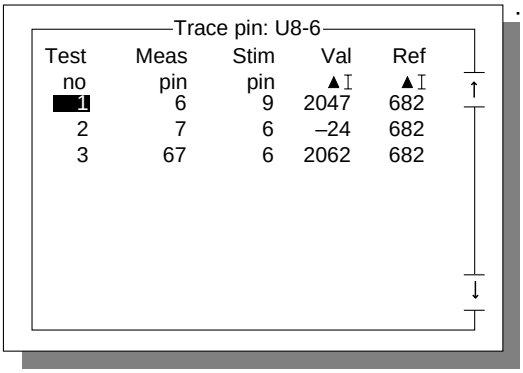
- **fails< comps>< pins>**

  Click to display the previous (left) or next (right) failed component or pin.

Worksheet in Action Once a test starts, the Status column shows pass/fail values.



Clicking the word “Pass” or “Fail” in the Status column opens a Trace Pin pop-up window displaying which pin-pair tests have been run to verify the correct pin.



Deleting Pin Pairs Clicking a test number allows deletion of a pin-pair test. Deleting a pair causes DeltaScan to look for an alternate pin pair to test the current pin the next time a test starts. Deleting all trace pin entries on a pin that is passing before re-starting and bringing up the trace on the same pin again reveals different pin pairs used to verify the correct pin.

The “Ref ^I” field value can be changed as needed. It changes the Pass/Fail criteria for the current pin pair and interacts with the ratios in the test threshold. If you change the test threshold after editing the Ref ^I field, the field value changes to accommodate the ratio change.

Note: Repeatedly starting tests, then bringing up trace pins and deleting all pin tests, eventually exhausts the ways to check that the current pin is not open. When that happens, the pin status changes to Unstable, and the pin becomes non-editable. The only way to rework the pin is to start over by re-validating the chip.

Review Board Fault Coverage

After validating the tests, generate the Board Fault Coverage report to see if the actual test coverage matches the predicted test coverage of the Analysis report you generated in the beginning. To create the report, select Board Fault Coverage from the Utility menu.

Fault Coverage for Board:
Board Directory : C:\TPD\UBSDOT - ICT
Date : Tue June 15 13:29:27 1998

Device Fault Coverage Data:

Device ID	Device Name	Fault Coverage Technique	Pins Analyzed	Pins Tested	Fault Coverage
U10	74FCT273	DeltaScan	17	17	100.00%
U11	EEPAL	DeltaScan	16	14	87.50%
U19	74F245	DeltaScan	18	18	00.00%
U2	RAM	DeltaScan	29	12	41.38%
U20	9346	DeltaScan	4	4	100.00%

Scroll through the report until you come to the DeltaScan tests. Look for discrepancies between Pins Analyzed and Pins Tested and for low percentages in the Fault Coverage column. Compare coverage values to the original analysis.

Problems you find may be the result of incorrect or incomplete topology or inadequate pin pairs for the test.

Edit the DeltaScan Database

After you have created a database, you can check its contents using the DTRAN.EXE program. To run, type at the MS-DOS prompt:

dtran dump <input-file> <output-file>

The dump file is an ASCII representation of a DeltaScan database. A newly generated database has no test information, only component information. To view test information, repeat the dump process after you have run Validate.

The Validate process makes measurements on the board under test to identify the best way to test each device lead. The results of this process are stored in the DeltaScan database. The database file itself is a binary file, but the dump utility creates an ASCII version of the database.

```
Board fault coverage: 96%

Deltascan Id: U10
Name: 74FCT273
Db reference: 1507328
Pin count: 20
Measurement ref: 340
Test threshold: Fixed 50
Learned threshold: 100%
Enabled: coverage 16/17 = 94%
Validated: Yes

Pin  Node  Type       Stim-pin/delta-I pairs
-----------------------------------------------------------------------
 1   211  Ignore     13 2156 17 2153   4 2147  16 2150 14 2151 12 2151
 2   206  Normal     3 2150  11 2158  17 2148  12 2161  14 2162  13 2155
 3   325  Normal     6 2162   1 2173   5 2151  16 2158  19 2155  15 2155
 4   313  Normal  16 2162   6 2161   5 2162   1 2163  19 2157  15 2158
 5   246  Normal  14 2157  15 2164   4 2157   7 2162  12 2159   3 2157
 6   260  Normal  12 2158   4 2159  14 2152   3 2156  19 2156  16 2153
 7   314  Normal  19 2159   2 2151   6 2161   5 2160  16 2158  15 2065
 8   303  Normal  15 2056   2 2162   6 2153   5 2168  16 2155  19 2081
 9  9999  N/C
10     0  Gnd
```

DeltaScan Database Each DeltaScan device has a record in the database.

Header Fields

- **Device**

  Device ID

- **Pin count**

  Number of pins on the device.

- **Measurement ref**

  Corresponds to the reference node in the worksheet. Check that the Measurement ref connects to the device ground pin only when the board is pulled down on the fixture.

Note: DeltaScan does not work well with devices such as op amps that have no ground pins; for such devices, use a local reference that is the device's most negative rail.

- **Test threshold**

  Corresponds to the test threshold selected in the DeltaScan worksheet.

- **Enabled coverage**

  The percentage of signal pins that DeltaScan is able to test. Power and ground pins are excluded from all coverage calculations. Device power pins do not participate in DeltaScan tests. The DeltaScan test method inherently depends on having a connected ground pin, so an open ground pin should indict all tested pins.

Device Pin Fields After the device header, the dump file lists the actual test for each pin. The tests are listed in device pin number order.

Pin Status Each pin record lists the pin number, followed by the tester node number connected to that pin, followed by the pin status:

- **N/C**–The node number is 9999 (not connected)
- **Power**–Device power leads or pins connected to a power pin.
- **Ground**–Device ground leads.
- **Tied Power**–Pins tied to power pins.
- **Tied Ground**–Pins tied to ground pins.
- **No Signal**–DeltaScan's LEARN was unable to find any pin pair that produced a large enough measured signal to use in testing the listed pin.
- **No Path**–The topology of the board is such that no other pin exists on the device which does not connect to same device(s) as the identified pin, therefore DeltaScan cannot produce a test for the pin.
- **Tied**–This pin is connected directly to another pin on the same device. DeltaScan does not make tests for tied pins. Called "Linked" in earlier versions.
- **Unstable**–The pin is not tested because DeltaScan's learn could not make a repeatable reading.
- **Normal**–DeltaScan's LEARN was able to find at least one way to test the pin.

Pins with Status of Normal Most pins identified as "Normal" are followed by a list of numbers which identify the pins and learned data found when measuring the pin. The numbers list the device pin used as the stimulus pin and the measured result when testing the pin.

A pin is likely to have several Stim Pin/Learn Data pairs. The pair with the strongest signal is usually the first in the sequence. If it is not the strongest, it may be first if the test is needed for testing one of the pins in the pair.

If the first measurement passes, the other tests do not execute, since the connections for the measured pin and stimulus pin have been verified. By providing multiple means for testing a pin, DeltaScan minimizes sensitivity to device variations and produces increased diagnostic resolution.

Failure Diagnosis to the Pin Since DeltaScan tests use pin pairs, having more than one test per pin allows failure diagnosis to the pin. If a pin has no numbers following "Normal," then that pin is configured only as a stimulus pin during DeltaScan measurements. You will see that pin used in testing other pins.

Lack of pin pairs does not necessarily mean that a pin is poorly tested: a pin used exclusively as a stimulus can be well-tested, provided it is used with several pins. Using a pin for stimulus is just as valuable as using it for measurement.

Database Analysis When you examine the database report, keep the following in mind.

- **Duplicate Component Entries**

  Duplicates in the database are a common cause of zero coverage steps. If you find duplicate DeltaScan component entries that are causing "no path" problems but are not visible from your DeltaScan section menu, you must delete all DeltaScan component entries. Then delete the DSCAN.DB file and start over.

- **Low Fault Coverage**

  For devices with low (<80% is a reasonable number) fault coverage, you can add a comment to the device summary describing why DeltaScan may have had trouble testing the device. Refer to the original Analyze report for help in understanding these results.

There is useful data in the link/leak data part of the analyze report. *Link* data lists what nodes DeltaScan determined to be in continuity. *Leak* data lists the nodes that fall within the given impedance ranges. Note that “R” means Ohms. (that is, 50–100R means 50 to 100 Ohms between the given nodes.)

- **Learn Threshold**

  You can make some judgments on the quality of the tests performed on the device by looking at the Stim Pin/Learn data for the device. The magnitude of the Learn data is one indication. The Learn data is the actual value measured during Validate. Validate uses the learn threshold to determine if a pin pair produces enough signal for a valid test. When the learn threshold in the worksheet is set at 100%, a measured value of 150 is the minimum that DeltaScan Validate accepts. In the worksheet, you can select 200%, 100%, 50%, or 30% as the learn threshold.

- **Test Threshold**

  The test threshold determines pass or fail when you run DeltaScan tests. In the DeltaScan worksheet, you can select High, Nom, Low, or the preset value for thresholds. Respectively, these set the acceptable test value at 1/2, 1/3, or 1/4 of the learned value, or at the preset value. You can control the minimum signal that DeltaScan includes in the test by changing the Learn threshold in the worksheet. You can change its sensitivity during test by changing the test threshold for the whole or by editing the data for a single pin pair. Pin pairs with larger signals are more likely to produce reliable tests than those with signals nearer the minimum. Sometimes, for pins with very low learned data, you may find it necessary to disable the pins in order to get reliable test results.

- **Number of Test Passes**

  Another indication of test quality is the number of test cases for a pin. A better test has more entries for testing the device, giving DeltaScan a bias toward passing good boards, and eliminating false failures: only if all tests in the list fail is the pin reported as open. This provides better reliability in production than using only one test case. Some devices have few test pins available because of board topology. For example, RAM devices are likely to have most pins connected to a single IC, reducing the pins available to DeltaScan for testing. As a result, the address and data pins are all tested using the only available unique pin—the chip enable. Tests of this type suffer in two ways: there is only one means to test a pin, and the only available means may have a fairly low signal.

Database Modifications By using the DTRAN.DMP mechanism on a previously validated test program, you can modify or add pin-pairs to a database.

Note: This feature works only on the current revision of the DeltaScan executables. It does not work with earlier versions of DeltaScan.

- **To generate the database report:**

  1. At the DOS prompt in a separate DOS window (not the 18xx DOS shell), type:

     dtran dump <output_filename>

  2. In the output file, modify pin pairs and test thresholds.
     - To add a new pin and threshold value, type the pin number and value before or after any of the pin/thresh pairs.
     - To delete a pin and threshold value, delete the pin number and threshold value.
     - To disable the entire line, type “Ignore” as the Type.
     - DTRAN.DMP recognizes only Normal and Ignore as valid types. You cannot change or create Gnd or NC.

3 When you have made your changes, import the modified file into your test program directory by typing:

dtran dump -o import <output_filename>

Note: If you perform DTRAN.IMPORT from within the 18xx DOS shell, you are likely to run out of memory.

Frequently Asked Questions About DeltaScan

Question	Answer
How well do DeltaScan results correlate with predicted fault coverage?	DeltaScan results should correlate extremely well with predicted fault coverage. If they do not, investigate problems using the troubleshooting table below.
How well does DeltaScan work across different manufacturers and different batches of components?	Test reliability is usually not a problem because DeltaScan's test technique is highly tolerant both of different manufacturers and of different batches, allowing you to add tests and devices to an existing database. Using Validate with append allows limits to accommodate variations.
What is DeltaScan's run speed?	Approximately 1.2 mS per pin
How do I know the reference node is wired properly?	Verify that reference nodes are only connected to ground when the DUT is in contact with the bed of nails.
What should I do if I use all eight DeltaScan pins?	Use relays on the Relay Array Board or enable G-Pole grounding.
Can I test analog integrated circuits?	You need a device substrate to tie to the board ground. This is usually not true for op amps, but may exist in other parts. However, if the negative rail is used as a local reference node, DeltaScan may work with op amps. Some analog devices are built using a dielectric isolation process which produces very low bias and leakage, with no parasitic or protection diodes; such devices cannot be tested with DeltaScan.

Troubleshooting Guide

Problem	Causes	Solution
Intermittent failures	Ground reference node incorrectly wired.	a) Wire the ground reference to a nail contacting the board ground trace. This nail should have no other wires attached to it. After you create a DeltaScan fixture, test the integrity of the ground reference by removing the test board, then select Start and verify that the system gives an error message. b) With board removed, node-find the reference node. You should only find the reference node.
	Fixture Contact	Verify good contact on board and fixture. Look for patterns, such as a particular node failing several tests. Does cycling vacuum affect results?
False passes	a) Ground reference node incorrectly wired.	a) Correct the wiring.
	b) Power supply not wired to a DeltaScan pin.	b) Correct the wiring.
	c) A component is on the board but not in the board database, so DeltaScan doesn't know about it.	c) Add component to test program and re-validate DeltaScan.
	d) Incorrect node.	d) Correct the nodes either on the DSCAN worksheet or in the input list, then regenerate and re-Validate.
Can't learn a pin	Validate messages:	
	a) No signal: DeltaScan couldn't find a large enough Delta signal given the constraints of the board.	a) The pin is not testable.
	b) No path: no unique pin is available.	b) The pin is not testable.
	c) Power or ground pin.	c) DeltaScan does not test power or ground pins.
	d) Unstable: pin is retested after you run Validate.	d) The pin is not testable.
	e) Tied pins.	e) DeltaScan cannot generate a test for a tied pin. All tied pins are counted as untested.
	f) No drive	f) Use worksheet "loop" control to find what signals are seen with these pins.

Problem	Causes	Solution
Results of Validate do not fall within the range specified by the analysis.	Topology, power, or fixture wiring (DeltaScan relays and/or the reference node) information may be incorrect or missing.	Edit the test program and revalidate.
Validate takes a very long time.	Incorrect or missing power information.	In the Dump report, check that the correct power/ground pin types have been assigned within each device.
Erroneous reduction of coverage (unstable tests or false passes or false fails).	Incorrect or missing power information.	In the Dump report, check that the correct power/ground pin types have been assigned within each device.
No power or ground pins listed for a given DSCAN test	Incorrect or missing power information.	In the Dump report, check the power section. Verify that each component has power and ground pins identified where you expect them to be. Pins listed as No-Signal or Unstable might really be power pins.
Erroneous increase of coverage (unstable tests, such as false passes or false fails).	Incorrect or missing interconnect and/or analog component data.	Add missing component data to the test program.

❖❖

CHAPTER 2 WAVESCAN

WaveScan detects opens on digital device leads without powering up the device and without applying digital vectors or Gray code. WaveScan uses magnetic inducers mounted over the device-under-test (DUT). An oscillating magnetic field induces voltages in conducting paths in the DUT, verifying proper connection.

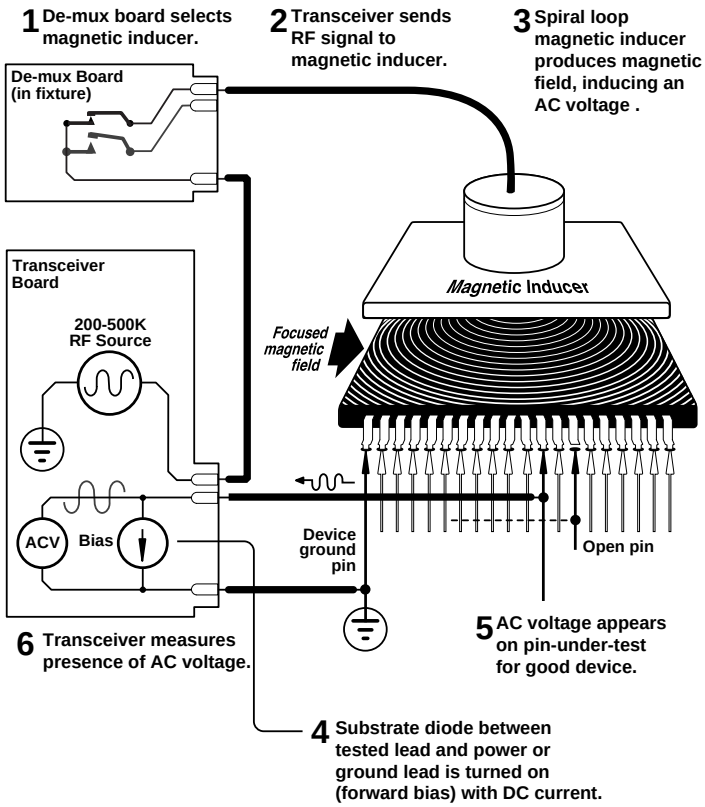
WaveScan is a Power-Off test for opens on the DUT.

Theory of Operation

WaveScan is based on the principle of magnetic induction, the mechanism through which transformers, coils, and relays operate. Magnetic induction occurs when a magnetic field changes around a conductor or a conductor moves through a constant magnetic field. The moving magnetic field induces an electric current in the conductor.

WaveScan uses a special magnetic field generator, called an inducer, which produces a magnetic field that changes with changes in radio frequencies (RF). This inducer is located directly over the device-under-test (DUT) and induces a small AC current in the unpowered device's conductors. A closed path for this current is formed by the die, the bond wire, a power or ground device lead, a tested lead, and the tester through the bed of nails.

In practice this path cannot be completed unless the substrate diodes between the tested lead and the power or ground lead are turned on. These diodes are turned on by applying a small DC bias current. The power or ground lead is tied to tester ground, and the AC voltage drop caused by the induced current is read between the tested lead and tester ground.



Executing a WaveScan Test

WaveScan executes tests in the following sequence:

- Calibration
- Pin test

Calibration

WaveScan software executes WaveScan calibration at the beginning of the WaveScan test section, prior to any WaveScan test steps, each time you select Start from the WaveScan worksheet, or during the program or section Run.

WaveScan calibration checks for the presence of RF noise at its normal operating frequency, and may adjust the frequency to avoid a large noise source very close to that frequency.

Note: If no usable quiet frequency is found, an error message will appear. It may be necessary to find and remove nearby sources of RF noise.

Pin Test

After the WaveScan software executes calibration, it begins to test pins. To test a pin of a device, WaveScan connects the F-pole to the node connected to that pin, the E-pole to the reference node, and all other nodes to the G-pole. The bias level is set according to the worksheet. The demultiplexer is switched, not to the inducer over that device, but to the auto-zero assembly. WaveScan makes a measurement using an integration time suitable for the threshold given in the worksheet. Then the inducer for the DUT is switched on, and the measurement is made again.

The first measurement is used as an auto-zero correction to the second to help compensate for any unavoidable crosstalk between the WaveScan transmitter and receiver, particularly with demultiplexer boards mounted in fixtures. This procedure cannot eliminate crosstalk entirely, and typically such crosstalk, rather than external or internal random noise sources, limits WaveScan sensitivity.

Note: The noise reading is not taken when Fast Mode is activated in the worksheet.

If the threshold level on a given lead is under 200, WaveScan repeats the measurement a few times and averages the results.

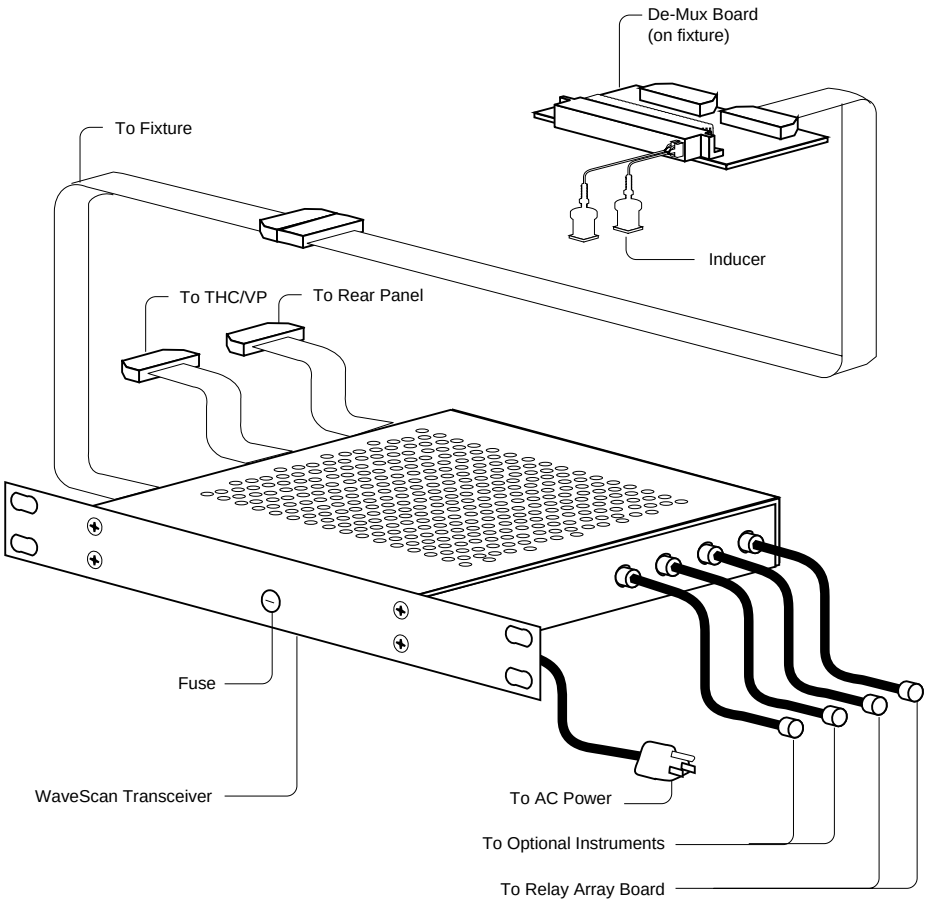
WaveScan Hardware

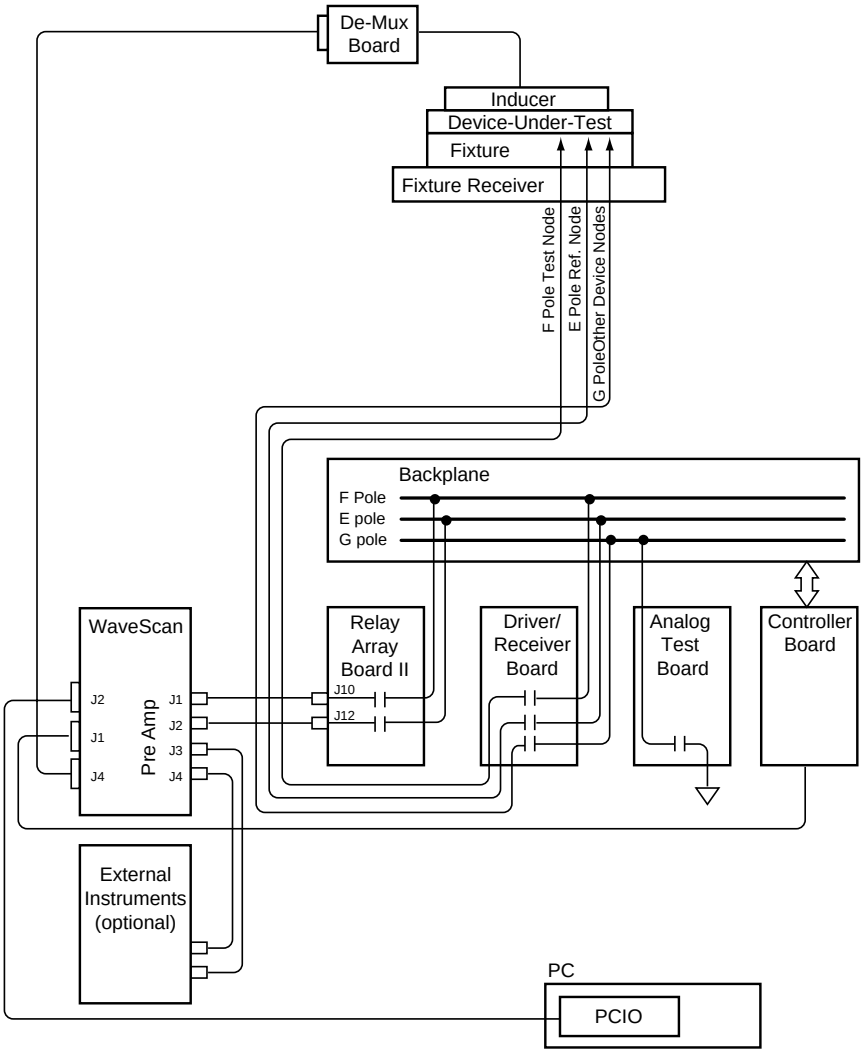
WaveScan hardware consists of:

- Transceiver consisting of transmitter, receiver, and power supply.
- Fixture-mounted demultiplexer board for selecting the inducers and a WaveScan magnetic inducer over each device to be tested.

The two diagrams below illustrate the WaveScan hardware and show a simplified interconnect diagram.

Information on specific fixture wiring can be found in the **Z1800-Series Fixturing Guidebook**. For information on running the WaveScan self-test, refer to the diagnostic chapter in the **Z1800-Series Maintenance Reference**.





Transceiver

The transceiver (PN 047-227-00) consists of:

- Transmitting instrument to generate a low frequency RF signal (387 to 587 kHz) that goes to the inducers
- RF receiver to measure AC voltage
- Bias current generator
- Power supply for the transceiver that also powers the demultiplexer(s)

Transmitter

The transmitter provides drive to the inducers. It uses a simple frequency synthesizer to tune the transmitter from 387 to 587 kHz. The transmitter delivers about half a volt and 50 mA rms inducer drive for each output, in-phase and quadrature. An inducer contains two sets of coils, driven in quadrature phase, to eliminate open “dead spots” in the magnetic field. To help preserve isolation between the transmitter and the receiver, the transmitter output is balanced, delivering the inducer drive on two twisted pairs of wires. The drive is delivered through the fixture cable and demultiplexer board to each inducer assembly, reducing the electric and magnetic field leakage to a very low level. The receiver can measure the current flowing in each transmitter output pair. The diagnostic and fixture

checking software can detect whether the transmitter load is that of a properly connected inducer.

RF Receiver

The receiver is a sensitive integrating receiver synchronized with the transmitter. The receiver is capable of measuring signals of less than 1 µV while signals as high as 3 mVrms will not overload it. The receiver input is connected differentially between two input connectors on the WaveScan transceiver. The input connectors are cabled to the E and F matrix poles via the Relay Array Board (RAB). The receiver provides loop-through for these connectors, terminating in SMA connectors, so you can still use external instruments which ordinarily would connect directly to SMA connectors on the RAB. The receiver is AC-coupled to the transceiver inputs. The bias sources inject DC current into the inputs. The DC current flows out to the DUT pin being tested. The inputs are clamped to within ±2 diode drops of each other. The E-pole connection (the reference node) is clamped within 2 diode drops to ground, preventing the bias sources from generating excessively high voltages. A DC meter circuit in the transceiver measures the DC bias current.

When a measurement is required, WaveScan software triggers the integrating receiver. Integration takes place for a certain number of transmitter cycles set by the software. The software reads the integrated value for in-phase and quadrature components from the converters. A busy flag in the software detects that integration is complete, at which point the software computes the magnitude of the induced voltage. For noise rejection, a differential measurement is made between the test lead and the reference node in the fixture.

Bias Current Generator

The transceiver has two bias current sources which supply up to ±20 mA each. These bias current generators turn on the DUT substrate diodes.

Demultiplexer Board

The demultiplexer board (PN 051-016-00) is the part of the WaveScan-equipped fixture that switches the RF signal from inducer to inducer as required by the WaveScan test.

A 26-pin ribbon cable from the WaveScan transceiver to the fixture powers and controls the demultiplexer board from the WaveScan transceiver. The cable has low RF leakage, achieved by balancing the inducer drive on two wire pairs. Additional signals in this cable allow the WaveScan transceiver to control the selection of the inducer.

Each demultiplexer board except the first can accommodate up to 32 inducers, and can be chained to additional demultiplexer boards up to a limit of 255 inducers. The first inducer location on the first demultiplexer board is reserved for the auto-zero assembly, a resistor block used to simulate an inducer load for calibration. The first inducer location available for an inducer in the fixture is inducer number one.

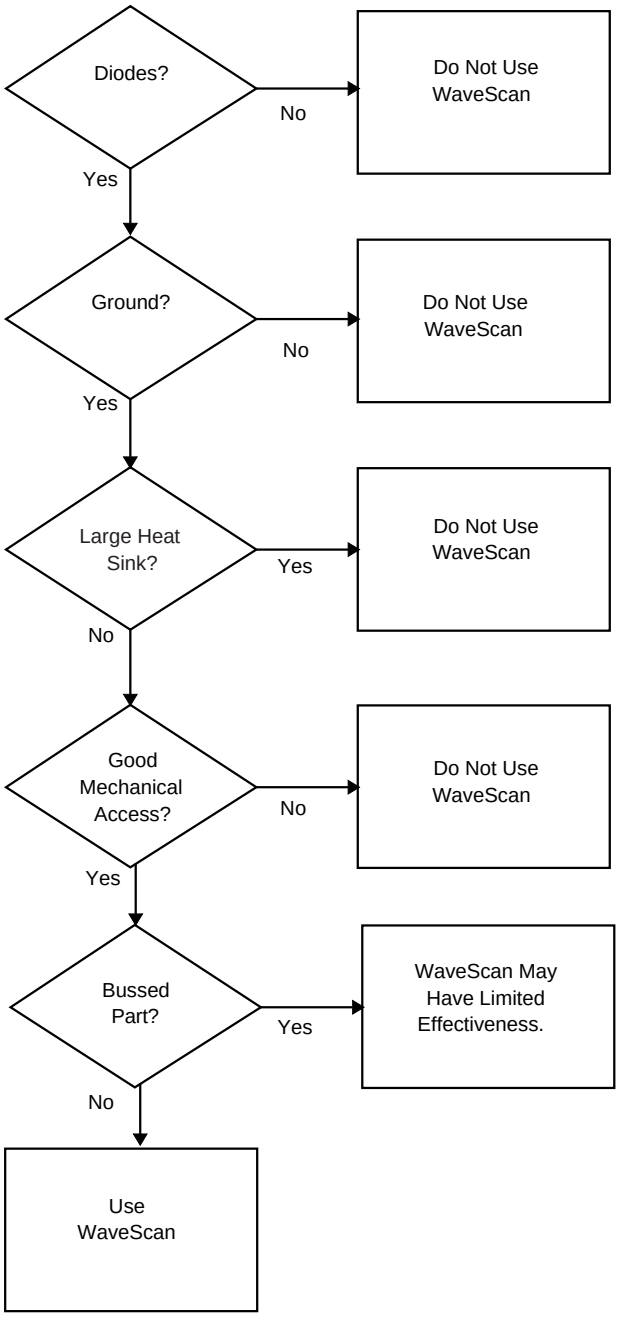
Inducers

WaveScan inducers are spiral inductive antennas formed on printed circuit board material. They are mounted in the fixture above the devices targeted for tests on the board under test. The inducers may be attached to an overclamp or they may be in the probe plate beneath the DUT.

When to Use WaveScan

WaveScan is a technique that detects opens on digital device leads without requiring digital vectors or Gray code. A WaveScan test is most appropriate for integrated circuits that have substrate diodes between input/output leads and power or ground. WaveScan is particularly useful for testing devices where knowledge of the device internals is limited. It requires a bed-of-nails pin contact on each device lead to be tested. In addition, WaveScan has only limited effectiveness testing bussed parts.

The flowchart below may help determine if WaveScan is appropriate for testing a particular device.



WaveScan Requirements

Before you can create a WaveScan test, you must define power, ground, continuity groups, and the MultiScan reference node.

Power and Ground Definitions

Define power and ground either in the IPL.DAT file using PWR and GND records, or by building a power test in the Brd_Pwr section of the worksheet. For WaveScan tests, power and ground definitions are required before generating a test.

Continuity Groups

Define continuity and jumper tests either in the input list or by building a continuity or jumper component test. For WaveScan tests, continuity group definitions are required before you run Generate. During a WaveScan test, the tester connects all nodes to ground except the MultiScan Reference Node, the node being tested, and any nodes connected to the node being tested. WaveScan uses information in the Interconnect section to identify nodes that connect to the node being tested.

MultiScan Reference Node

Establish a MultiScan Reference node if one does not already exist. The transceiver uses the reference node to cancel noise from the signal. The reference node is stored in the Header/PRGMVARS step in the MultiScan Reference Node field. It should appear in the MultiScan Reference Node field, not in the list of Ground Reference Nodes. The reference node default is 9999.

The reference node default in the PGEN.CFG file is 9999. You can specify the reference node by editing Header/PRGMVARS or PGEN.CFG file, as explained in “Update PGEN.CFG” on page 2-11.

Selecting a Reference Node

The reference node must be an unused node. It occupies a single tester node. You must define a single reference node to be used for all WaveScan tests. The reference node must connect to the ground bus of the board under test. The node you enter must be the same node as is wired in the fixture. Although you can use any valid unused tester node number as the reference node, we recommend that reference nodes be chosen from available Sense nodes. If the program uses the G-pole for power-supply grounding, the reference nodes must be chosen from available Sense nodes.

The reference node must be in a different 16-node group from the device ground and from any power supply. For example, if you have a device ground at node 0, put the MultiScan Reference at node 16. Do not use the system ground node 0 as the reference node. Use node 16 when possible.

Checking Reference Node Wiring

You may need to verify that the reference node is wired correctly (for example, if device test failures are intermittent). For this test, Teradyne recommends that you choose an available sense node from the fixture interface. This means that the node is in the upper 16 node group of the D/R board. Any power supplies connected to the same 16 node group on any D/R board cannot use G-Pole shorting for grounding.

The fixture probe that contacts the board ground should have only a single wire on it. The wire connects the DUT board ground to a node in the tester. A common error in wiring the reference node is the addition of wires to the fixture ground plane, V reeds, or DUT power supply. Record the reference node you have established for later use during program generation. This reference senses ground at the board under test. Establishing the proper reference node is mandatory for dependable FrameScan results.

WaveScan PRGMVARS

Header/PRGMVARS includes the following General and Report variables important to WaveScan testing. If you use WaveScan, check these variables.

For a description of all fields in Header/PRGMVARS, refer to the **Z1800-Series Programmer's Guidebook**.

```
18xx Windows mode-init_com
Edit   Save   Revert   Quit
                                  Header                                [ ↓ ]-[ ↓ ]
( √ )  General Variables   (  )  Report Variables
                              General Variables
 Vacuum Select            : Vacuum 1      Vacuum Delay (mS)        : 100
 Auto Probe Check (APC):  Off             Stop On Fail (SOF)       : Off
 Digital HiCheck          : Off           Skip On Fail             : Off
 Digital Tracer           : Off           Backdrive Timeout (mS)   : 0.0
 Section Abort            : On            Duty Cycle (%)           : 0
 Abort On Fail Count      : 0             Learn Cap Phase Offsets  : Off
 Discharge Method         : DschrgSect    DR1 Emulation            : Off
 MultiScan Discharge      : On            DFP Configuration        : Off
 Power Down Sequence      : Reverse       External Power Down      : Off
 Ground Reference Nodes  (      ) (     ) (     ) (     ) (     )
W MultiScan Reference Node ( 340)   FrameScan Plus Measure (99)
 DeltaScan, Short Pwr/Gnd via G-pole:   Off
 DeltaScan, Verify Pwr/Gnd Shorting:    Off
 DeltaScan, Fixed Threshold:            50

 Board Description        [                                                ]
 Dscan retry              [5 ]        Dscan retry delay          [  1] ms
 Dscan Run ALL Pin Pairs  On          Dscan Hard Fixed Thresh  [Off]
Dscan will run all posible pin pairs for data collection
C:/TPD/DEMO\DEMO_172 - ICT    START    CANCEL    SOF   HLD   RPT   CRT
```

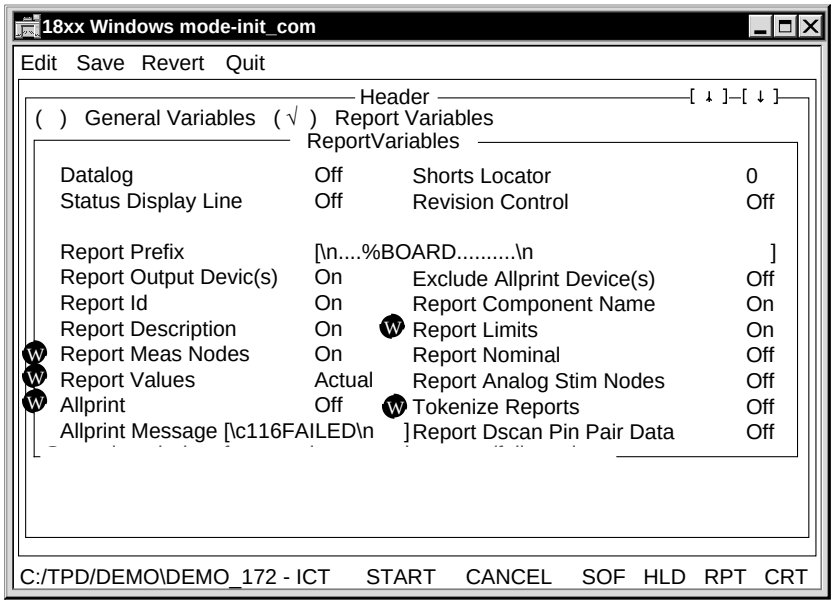
W WaveScan variable

General Variable

- **MultiScan Reference Node**

  Senses the actual ground level of the board under test.

Note: The default MultiScan reference node in the PGEN.CFG file is 9999. You can specify the reference node by editing the PGEN.CFG file before generation or entering the reference node in Header/PRGMVARS at any time.



WaveScan variables

Report Variables

- **Report Meas Nodes**

  Off: The pin number is included in the report, but the node number is not included.

  On: The node number is included after the pin number in the report. The report includes one line per failing pin.

- **Report Values**

  Off: The report does not include any of the measured values.

  Actual: The report includes the actual measured values.

  Percent: If you select percent, the report includes actual values, since FrameScan Plus tests do not report percent.

  If Report Values is Actual or Percent the report includes one line per failing pin.

- **Report Limits**

  On: The report includes the Pass/Fail limits of the test.

- **Allprint**

  On: A report is generated for every test, not just the failing tests.

- **Tokenize Reports**

  On: The Datalog and CRT reports are in Tokenlog format. The report file is TOKENLOG.DAT and is in the TPD\PROGRAM directory.

Developing a WaveScan Test

This section explains how to add WaveScan tests to a new board test program.

- **To develop WaveScan tests:**

  1. Set up WSCAN tokens.
  2. Update the PGEN.CFG file.
  3. Generate tests.
  4. Validate and troubleshoot tests.

Adding to an existing board test program To add a WaveScan test to an existing board test program, follow the procedures outlined in the **Z1800-Series Programmer's Guidebook** for incremental test generation.

Note: If board topology has changed, run PGEN/Learn to reestablish the continuities, special cases, shorts, and merged special cases on the board.

Set Up WSCAN Tokens

The input list (IPL) is an ASCII file that contains a complete description of the board component parts and interconnections. For each WaveScan test, modify the IPL syntax by adding an input list record to support the WaveScan test type.

IPL Record

A record is a section of the input list file IPL.DAT dedicated to a single component test step. Like all other component tests, a WaveScan test is governed by its input list record.

Record syntax for a WaveScan test:

Token	ID	Description	Name	X Inducer	Node List
`WSCAN,`	`U1_WS,`	`"WaveScan Test",`	`PAL22V10,`	`X17,`	`33,17,16,15,14`

Major and Minor ID Follow the Major/Minor ID convention for all components tested with both FrameScan and other tests methods.

- The major ID is the part of the ID that comes before a dash or hyphen (-) or an underscore (_).
- The minor ID is any part after the major ID, including the dash or underscore.

In P1_A, for example, P1 is the major ID and _A is the minor ID. Add a unique minor device ID to each new component entry. For example, use _FS, so that P1 becomes P1_FS. The major device ID, P1, will not be in conflict with P1_FS.

Inducer Number The inducer number specifies which inducer to use for the component to be tested. You must type an x in front of the inducer number to distinguish it from the node numbers.

Node List First node in the list is the first pin on the device, second node is the second pin, and so on for each pin on the device up to 625 pins. Use the number 9999 for an unconnected pin.

Refer to the **Z1800-Series Programmer's Guidebook**, Chapter 7, "Program Generator Tools," for more information about record syntax in general.

Update PGEN.CFG

Settings in the PGEN.CFG file configure the program generate function. You can edit the PGEN.CFG file to specify other WaveScan test default values for PGEN to use instead of the standard defaults. For a complete discussion on editing the PGEN.CFG file, refer to the **Z1800-Series Programmer's Guidebook** Chapter 7, "Program Generator Tools."

The following fields in the PGEN.CFG file apply to WaveScan.

- **DISABLEPWR**

  Defining power leads is required for a WaveScan test, but defining the leads normally causes generation of a power test.

  Disable power disables the automatic generation of a power test when power nodes are defined.

  The DISABLEPWR default is No. If you don't want to execute any power tests, set DISABLEPWR to Yes.

- **MSCANREF**

  MultiScan Reference Node is an otherwise unused node that lets you specify the reference node for a WaveScan test. The MultiScan reference node is stored in the Header/PRGMVARS worksheet of the test program for the board.

  Although the default is 9999, the value must be set to a valid reference node. You can specify the reference node by editing the PGEN.CFG file before generation or entering the reference node in Header/PRGMVARS at any time.

  PGEN adds this node to the Header/PRGMVARS Multiscan reference node field during incremental program generation.

- **WSCANBIAS**

  WaveScan Measurement Bias specifies the bias current used to bias the substrate diode for a WaveScan test. The range is -20 mA up to -2 mA, and 2 mA up to 20 mA, in 1 mA steps. The default is -10 mA.

- **WSCANTHRESH**

  WaveScan Measurement Threshold specifies the measurement threshold in tenths of a microvolt. The program generator uses this value in generating a WaveScan test. For a pin to be detected, the measured value must be higher than the threshold.

  Values may be from 1 to 32,000. The default is 100 (10 µV).

Build the Database File

Once edits are completed, save the IPL, and continue with these steps:

- **To build a new board test:**

  1. Run **PGEN/CLEAN**.
  2. Run **PGEN/BUILD.**

     This command creates a new temporary IPL database, IPL.DBF.

- **To build an existing board test:**

  Do NOT run PGEN/CLEAN. Run **PGEN/BUILD**.

  If you accidentally select PGEN/CLEAN, copy the board directory from your backup and start over.

Generate Tests

The PGEN/GENERATE command automatically generates the test program ICT.TST from the IPL. The process for developing and executing a test program that uses WaveScan is the same as the existing processes for developing a Z1800-Series test program.

The three test generation methods are automatic program generation, incremental program generation, and manual program generation. They are described in the **Z1800-Series Board Test Tutorial**.

Important: The Programmer Efficiency Package (PEP) does not recognize WaveScan tokens and will not perform an analysis on them in the input list.

- **To automatically generate a test:**

1. Run **PGEN/GENERATE**.

   This command adds the IPL.DBF entries to the main test program ICT.TST. Do not be concerned about messages regarding missing power or ground. Updating and subsequently running Validate eliminates such messages.

2. Run **PGEN/UPDATE.**

   This command is needed to finalize topology for all reports and before any Validates. The update is critical for success.

3. After generating WaveScan tests, review the resulting worksheets.

   Make sure that the Multi-Scan Reference node, thresholds, nodes, etc. have been set correctly:

Validating and Troubleshooting Tests

Use PGEN/VALIDATE and your own analysis of system worksheets and reports to achieve maximum test coverage and eliminate false passes, false fails, and unstable tests.

Make edits to the worksheets and the database, as needed, to improve the tests. Follow this process:

- Validate the tests.
- Look at the WaveScan worksheets and reports. Edit worksheets as necessary.
- Continue to run Validate and edit component and test attributes until you have the program perfected.

This section covers validating and troubleshooting suggestions, tools and processes. For complete information, also read Chapter 7, “Program Generator Tools” and Chapter 9, “Test and Debug Tools” in the **Z1800-Series Programmer’s Guidebook**.

Validate Tests

The Validate tool provides a way to learn test parameters from a known good board. Validate is required for WaveScan test development because the default biases and thresholds may result in some false failures. Validate is necessary to help select the correct bias and threshold for the conditions on the board.

- **To validate WaveScan test programs:**

1. Select **Validate** from the Setup menu.

   The system displays the Validate Configuration window.

2. Select **Validate WaveScan**.

3. In the **Threshold Variance Reported** field, specify the variation in tenths of microvolts the system uses to determine whether it will write a message into the EXCEPT.LST file when Validate changes the measurement threshold in a WaveScan test.

If Validate determines that the proper measurement threshold varies from the test page default value by a value that is greater than the test page default, it writes a message into the EXCEPT.LST file. It does not write a message if the variance is less than the default value.

The range of acceptable values is 1 to 255.

4 In the **Minimum threshold allowed** field, specify the minimum threshold Validate sets before changing a pin to Not Tested.

5 Run **Validate** from the WaveScan section or WaveScan component editor using a known good board on the fixture.

Prior to making any measurements, Validate runs the same calibration routine that is run when a test begins.

Validate generates a report listing each parameter it changed. The report goes to the exception list file, EXCEPT.LST. You can filter inconsequential changes from the report using **Setup/Validate/Validate WaveScan/Threshold variance reported**.

Note: If you are not sure of the quality of the available supply of boards used for Validate, you need to examine each WaveScan test, determine the cause of problems, correct them if possible, then re-validate.

6 Run **Validate** on additional good boards.

7 Troubleshoot any failures.

See the troubleshooting suggestions in the topics below.

8 Revalidate individual devices as necessary to get repeatable and stable tests on the sample boards.

MultiScan Failure Flag A system flag called MultiScan Failure is set if any MultiScan test fails, including WaveScan. If the Section Abort feature is enabled, a failure causes the software to jump to the Trailer.

Troubleshoot Tests

This section contains suggestions for making test program corrections. Start troubleshooting by examining the test reports and worksheets.

Analyze WaveScan Output

In addition to the exception list file, EXCEPT.LST, WaveScan outputs Statistics (Fault Coverage), Datalog, and Tokenlog reports.

WaveScan Statistics Report WaveScan Statistics report indicates the fault coverage for the DUT. The fault coverage is a percentage, the number of tested pins divided by the number of pins included in the WaveScan Fault Coverage analysis. The number of pins included in the WaveScan Fault Coverage analysis is not necessarily the number of pins on the device.

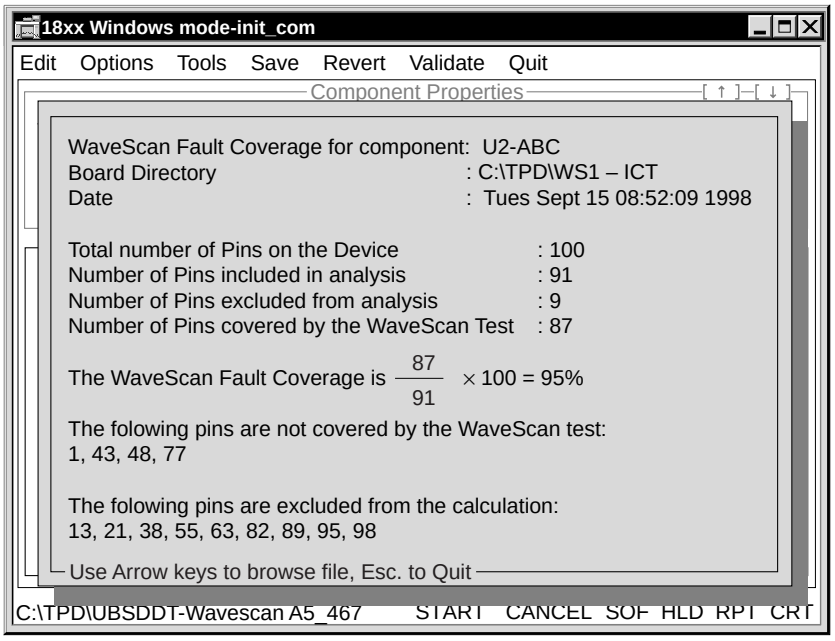
The Statistics report treats the pin types as follows:

Fault Coverage Contents	Pin Types
Pins covered and included in the analysis:	Normal
	Normal Tied
Pins not covered but included in the analysis:	Tied
Pins not covered or included in the analysis:	Ground
	Power
	Not Connected (N/C)
	Not Tested

- **To view the report:**

1. From WaveScan worksheet menu bar, select **Tools**.
2. From the pulldown menu, select **Statistics**.

   A window appears as illustrated.



3. Select **Esc** to quit the report display.
4. Save the report to a file. The system appends the extension .TXT.

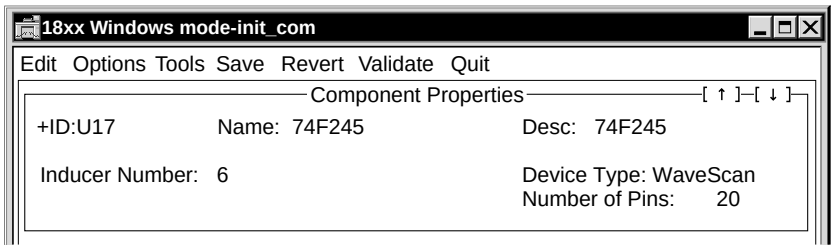
WaveScan Datalog/CRT Reports When you execute a WaveScan test, the software generates a report. If Allprint is On, the report includes both passing and failing test results. If Allprint is Off, the report is limited to failing tests.

WaveScan Plus Tokenlog Reports WaveScan test results will be logged by Tokenlog if you select Tokenlog in the Setup-Data-Program Execute channels window. If you select Tokenize Reports from PRGMVARS in the Header, the Datalog and CRT reports will be in Tokenlog format. The report file is TOKENLOG.DAT and is in the TPD\PROGRAM directory.

Edit WaveScan Worksheets

Use the fields and controls of the WaveScan worksheets to troubleshoot tests.

Component Identifier Section The Component Identifier section of a WaveScan worksheet specifies the information required to generate a WaveScan test for a component. You previously set up the information by running Build and Generate on the IPL or manually adding a WaveScan component and filling in the information on the worksheet.



Component Identifier Fields

- **ID**

  Component identifier. For example, “U14.” The + preceding the ID indicates that the step is enabled.

- **Name**

  Device name.

- **Desc**

  Text description of the test. For example, “IC Pin Test.”

- **Device Type**

  WaveScan

- **Number of Pins**

  Total number of pins on the component (from 1 to 625).

  The Node Entry box pops up when you click on the number in the Number of Pins field.

- **Node Entry** (before generating test)

  Assign node numbers using one of the following three methods.

  - Via the input list and program generators
  - By probing the fixture using the node entry window and Nodefinder
  - By manually editing the node entry box

  Use the node number 9999 to indicate an unconnected pin. As such, 9999 becomes a place holder for the node number location.

- **Node Entry** (after generating test)

  If you edit nodes after you generate the worksheet, you must change any 9999 nodes to N/C (Not Connected). Each pin marked Normal or Normal Tied must have a legal node number associated with it. The number cannot be 9999.

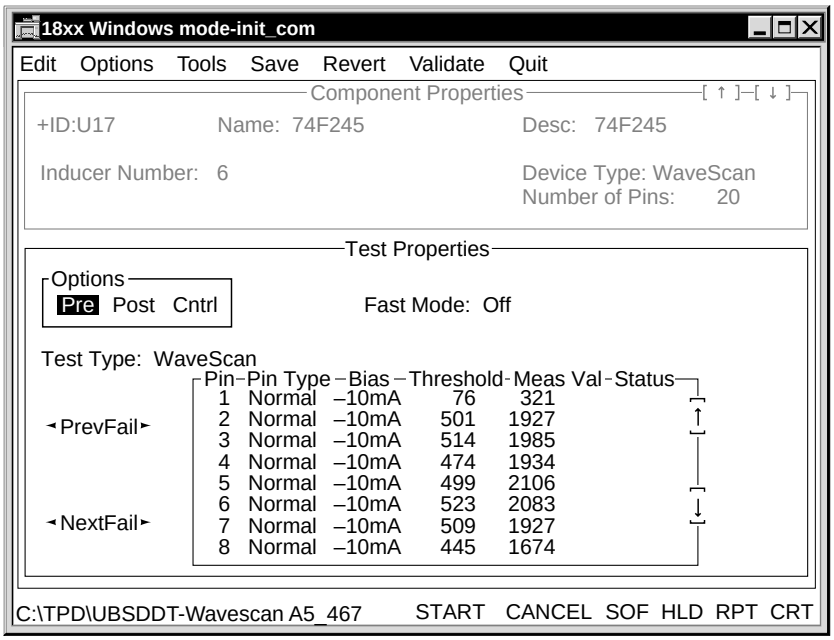
  The pin type for an unconnected pin cannot be Normal or Normal Tied. If you use 9999 as the node number for a Normal or Normal Tied type, WaveScan displays the error message:

  ```
  MultiScan: Device_pin_Specifies an out of range node number
  ```

- **Inducer Number**

  Enter an integer from 1 to 255 to indicate which inducer to use to stimulate the component being tested.

Test Properties Section The Test Properties section of a WaveScan worksheet displays test parameters and results. From here you edit and execute the test step.



Test Properties Fields

- **Options**

  Displays the Pre-Test, Post-Test, and Test Page Control options.

Note: Because the Z1800-Series system software does not regain control between WaveScan tests, relays and external programs are not available in the WaveScan worksheet pre- and post-test options.

- **Fast Mode**

  You can turn Fast Mode testing On or Off with this field. Fast Mode can be used in situations where test speed is important and testability is already proven.

Note: Fast Mode removes noise measurement and signal averaging from the test result, so its results may not be as stable as Normal Mode (Fast Mode Off) results.

- **Test Type**

  WaveScan.

- **WaveScan Pin Parameter Window**

  WaveScan Pin Parameter window allows you to specify the test parameters for each pin. You may specify the pin type, measurement bias, and measurement threshold. WaveScan software fills in the measured value and test status fields after the test is run.

  The Pin Parameter default values are:

  - Pin Type:Normal
  - Measurement Bias:-10mA
  - Measurement Threshold:10µV

The screen reflects the system resolution of tenth microvolts. For example, a threshold of 20.0µV appears as a value of 200.

You may enter information for up to 625 pins in the Pin Parameter window. Use the scrolling arrows at the right edge of the screen or the keyboard arrow keys to move through the screen.

The Prev Fail (previous) and Next Fail buttons at the left edge of the screen scroll the display to the previous or next failing pin.

- **Pin Type**

  The pin types are:

  - **Normal**. The pin is an independent signal pin.
  - **Normal Tied**. For each tied group, one pin has the Normal Tied pin type and all others have the Tied pin type. The tester measures a Normal Tied pin in the same way it measures a Normal pin. The Normal Tied pin will fail when all pins tied to the same node are open. If some of the tied pins are connected, the test may or may not fail.
  - **Tied**. The pin is tied to another device signal pin. No test is made for pins marked Tied. One pin is marked Normal Tied. WaveScan test results are reported for this pin, although the test results could indicate any or all pins in the Tied group. See the description for Normal Tied.
  - **Ground**. The pin is either a ground pin for the device or a signal pin tied to ground.
  - **Power**. The pin is either a power pin for the device or a signal pin tied to a power voltage.
  - **N/C** (Not Connected). The pin is either not connected inside the device package or is not connected to a nodal pin.
  - **Not Tested**. The pin is not to be tested. Validate changes pins from Normal to Not Tested when it cannot make a reliable measurement. Once a pin is marked Not Tested, Validate will not attempt to make a test for the pin.

- **Bias**

  The bias current is a small current applied to the device pin that is sufficient to turn on substrate diodes on digital devices.

  The measurement bias field specifies the current used to forward bias the substrate diode in order to measure the small AC voltage caused by the RF signal at the inducer.

  The measurement bias current range is +2mA to +20mA and -2mA to -20mA. For most devices either +10mA or -10mA produce the best results. The default is -10mA.

  If you consistently use a bias different from the default, you can change the value using the WSCANBIAS parameter in the PGEN.CFG file. Validate selects -10mA, 10mA, -20mA, or 20mA, selecting polarity that delivers the highest detected signal.

  Bias and Threshold are relevant only for Normal and Normal Tied pins. These fields are blank for other pins.

- **Threshold**

  The threshold is the minimum signal that indicates the presence of an induced signal rather than random system noise. To avoid cross-talk, the threshold is set higher if the received signal is higher.

  The measurement threshold field specifies the AC voltage used to determine whether a pin passes or fails the WaveScan test. If the measured voltage is below the threshold, the pin is determined to be open. If the measured voltage is equal to or above the threshold, the pin is connected properly.

The threshold range is 1 to 32,000. The default is 100.

Because Validate determines the optimum threshold values to use for a WaveScan test, usually you will not have to change any settings. However, if you would like to use a value other than that set by Validate, you may do so. You may type the new values into the worksheet after you have run Validate. You can change the default value using the WSCANTHRESH parameter in the PGEN.CFG file.

Bias and Threshold are relevant only for Normal and Normal Tied pins. These fields are blank for other pins.

- **Meas Val**

  This field shows the actual measured voltage of the pin in tenths of a microvolt.

- **Status**

  The Status field indicates whether the pin passed or failed the test. This field is blank unless the pin fails.

- **Prev Fail and Next Fail**

  Use the Prev Fail and Next Fail buttons to move from the current pin to the previous or next failing pin.

  Select the buttons by either clicking with the mouse or positioning the cursor on the button and pressing Enter. While you are in the pin parameter window, you can use the key combinations of Ctrl-Up Arrow to move to Prev Fail and Ctrl-Down Arrow to move to Next Fail.

Interpreting Measured Values When testing takes place, the receiver sensitivity is adjusted at each pin measurement so that the threshold is in the middle of the receiver's dynamic range.

- **9999—Good**

  If the measured signal is above the threshold and above the receiver limit, the worksheet displays the number 9999 instead of a measurement value and the pin passes. Passing is the correct conclusion, since a limiting signal is certain to be above the threshold.

  9999 readings indicate a large measured signal. If measured results change from a "real" value to 9999, it means the measured signal is near limits. 9999 signals are good.

  - To know what the level actually is on that pin, raise the threshold temporarily and repeat the test. The measurement will be repeated at a lower sensitivity.
  - To avoid false failures, keep the thresholds that Validate selected. These thresholds may result in the receiver reaching limits for many pins, and the Meas Val field displaying 9999.

- **8888—Bad**

  An 8888 result in the Meas Val field indicates that a large amount of noise is present for that pin. An 8888 display indicates a problem.

  The noise may be caused by the demultiplexer board being located too close to fixture wiring, producing too much crosstalk.

  - To correct crosstalk, place the demutiplexer board outside the fixture pan as far away from fixture wiring as possible. If you continue to receive 8888 readings, use shielded cable to connect to the demultiplexer board and shield the demultiplexer board inside a Mu metal box.
  - If the Meas Val field continues to display 8888 after shielding, change the pins reporting 8888 to Not Tested. Validate changes pins that have too much noise to Not Tested.

Changing the Bias and Threshold Fields for Pin Stability Validate affects parameters of the Bias and Threshold fields in the Test Properties section of WaveScan worksheet.

Validate finds the best of either -10, +10, -20, or +20 mA measurement bias for each pin. Validate determines whether -10, +10, -20 or +20 gives the best measurement for each pin, and selects an appropriate threshold for that measurement. WaveScan obtains results for -10 and +10, then for -20 and +20. If the signals obtained for 20 are significantly larger than those for 10, WaveScan uses the bias value of 20.

If Validate is unable to achieve signal level sufficiently high to allow a reasonable threshold, it changes the pin from Normal to Not Tested in the worksheet. If Validate finds a significant portion of the signal to be noise or crosstalk, it will change the pin to Not Tested.

Note: Bias and Threshold values are relevant only for Normal and Normal Tied pins.

Bias The DC bias current that WaveScan applies is shared by all the devices connected to the net which connects to the device pin being tested. For this reason the bias current flowing in the tested pin will usually be smaller than the bias current set in the worksheet. Furthermore, the voltage induced by WaveScan into the DUT will undergo a voltage division resulting from the equivalent resistance of the forward-biased diode in the DUT and the equivalent resistances of the forward-biased diodes in the other devices on the net. Protective diodes have characteristics varying over orders of magnitude from one device type and pin to another, causing a large range of signal variation from pin to pin on a WaveScan tested device connected to other devices.

- To correct a low detected signal, experiment with increasing the bias level to increase detected signal. Also, try both bias polarities to see which gives the best results.
- To correct unstable pins, a smaller bias value may be better. If a tested pin seems unstable, you may try lower values to determine if a larger signal level can be achieved.
- After editing the Bias, decrease the Threshold. Once the bias giving the most favorable combination of diode operating points is found, set the threshold in the worksheet to a value well under the received signal, for example, a fourth of it. If the received signal is reasonably high, the threshold will still be well above the level which would be received were the pin open. Validate assists with the otherwise tedious task of finding the best bias polarity and setting the threshold.

Threshold **If** failures occur, adjust some pin thresholds downward slightly.

When you reduce a threshold, verify that it is still above the noise level. To do so, raise the overclamp so the inducer is at least two inches away from the device or edit the worksheet to temporarily change the inducer number to the number of any other installed inducer, then run the test. All the pins should fail.

Removing Low Impedance Paths If a WaveScan-tested node has an impedance of 50 ohms or less to another node, you can include those nodes as a jumper or continuity so that the test node won't have a low impedance to ground. For example, if IC7 pin 4 has a 33 ohm series termination resistor to IC2 pin 4, include the resistor in the jumper section.

Note: Be careful that low impedance to ground is not confused with a ground pin.

Changing a "Not Tested" Pin Type Use care when changing a "Not Tested" pin type. In general, pins with a pin type of "Not Tested" should not be changed to any other pin type. Validate software changes the pin type to "Not Tested" for reasons such as:

- Too small a signal level
- Too high a noise level
- Excessive variation in signal levels

When you change a pin from "Not Tested" to another pin type such as "Normal," the apparent gain in fault coverage is acquired at the risk of producing false failures or false passes when the test is run. If you override Validate, run the test multiple times to ensure stability of the test.

❖❖

CHAPTER 3 FRAMESCAN

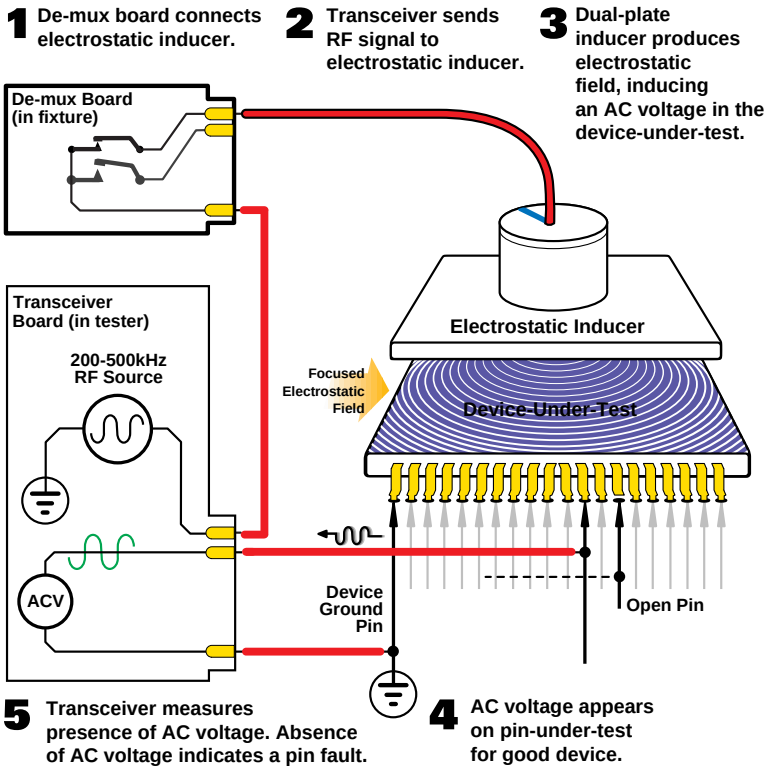
FrameScan is a technique that detects opens on device leads without powering up the device and applying digital vectors or Gray code. It also finds opens on connector or socket pins without making physical contact with the connector or socket. FrameScan uses electrostatic inducers mounted over the device-under-test (DUT). An oscillating electrostatic field induces voltages in conducting paths in the DUT, verifying proper connection.

FrameScan is a Power-Off test for opens on the DUT.

Theory of Operation

FrameScan employs the principle of electrostatic field coupling. When an oscillating electrostatic field occurs near an electric conductor, an oscillating voltage appears in the conductor. FrameScan measures the voltage changes, indicating any open connections.

FrameScan uses a special electrostatic field generator, called an inducer, which produces an electrostatic field that changes with changes in radio frequencies (RF). This inducer is located directly over the device-under-test (DUT) and induces, via capacitance, a small AC voltage change in the unpowered device's conductors. (Although a capacitive phenomenon is involved, capacitance is not measured.)



Executing a FrameScan Test

FrameScan executes tests in the following sequence:

- Calibration
- Pin test or Validate

Calibration

FrameScan executes calibration either at the beginning of the test section each time you select Start from the FrameScan worksheet, or during the program Run or section Run.

FrameScan calibration checks for the presence of RF noise at its normal operating frequency and may adjust the frequency to avoid a large noise source very close to that frequency.

Pin Test

After the software executes calibration, it begins to test pins. To test a pin of a device, FrameScan connects the matrix F-pole to the node connected to that pin, connects the E-pole to the reference node, and grounds all other nodes via the G-pole. FrameScan also closes the V-reeds on all DR boards to create a solid connection between the ground of the board under test and the tester's ground. (If FrameScan is used in a test, connect the V-pins even if no power-on tests are done.)

When Fast Mode is "Off," the demultiplexer is switched, not to the inducer over that device, but to the auto-zero assembly. FrameScan makes a measurement using an integration time suitable for the threshold given in the worksheet. Then the inducer for the DUT is switched on, and the measurement is made again.

The first measurement is used as an auto-zero correction to the second to help compensate for any unavoidable crosstalk between the transmitter and receive. This procedure cannot eliminate crosstalk entirely, and typically such crosstalk, rather than external or internal random noise sources, limits FrameScan's sensitivity. (Fast Mode skips this noise measurement.) If the threshold level on a given lead is under 200, FrameScan repeats the measurement a few times and averages the results.

Note: In Fast Mode, there is no averaging because only one measurement is taken.

FrameScan Hardware

FrameScan uses the same hardware as WaveScan, with the exception of using FrameScan inducers rather than WaveScan inducers.

FrameScan inducers consist of two metal plates separated by an insulator. They are mounted in the fixture above the devices targeted for test on the board under test. The inducers may be attached to an overclamp or they may be in the probe plate beneath the DUT.

The different inducers cause the transmitter portion of the WaveScan/FrameScan transceiver to behave differently in the FrameScan mode.

When in the FrameScan mode, the transmitter delivers about four volts (4V) to the driven plate of the FrameScan inducer. The drive is delivered through the fixture cable and demultiplexer board to each inducer assembly via coaxial cable, reducing the electric and magnetic field leakage to a very low level.

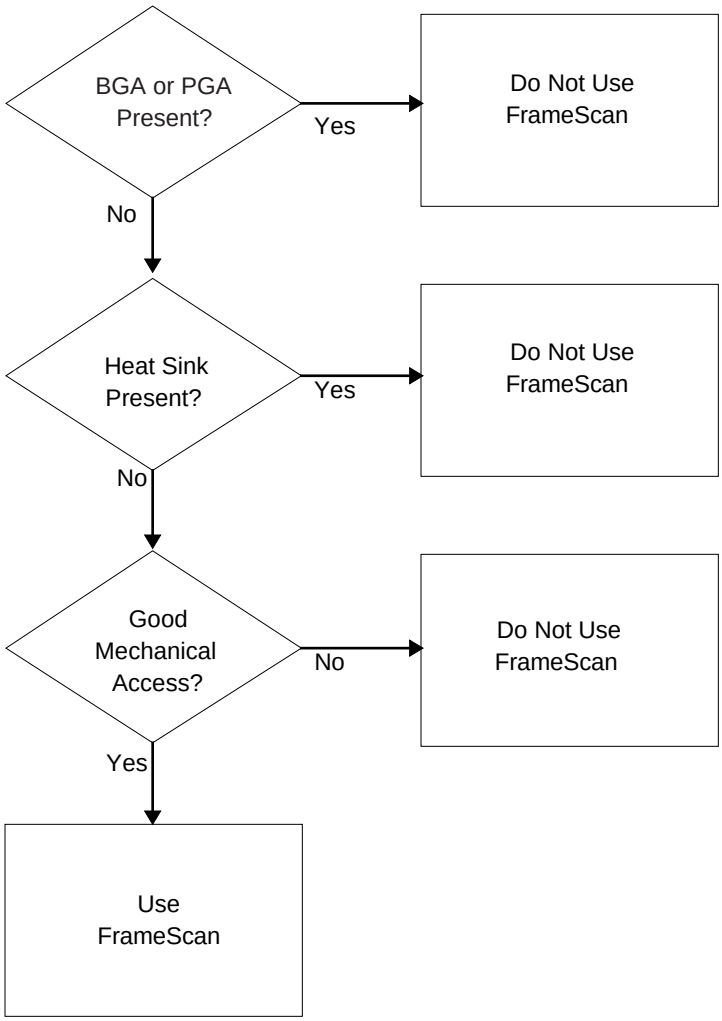
For descriptions and diagrams of the WaveScan/FrameScan hardware, see **Chapter 2—WaveScan**.

When to Use FrameScan

FrameScan is a technique that detects opens on connectors or on device leads, without requiring digital vectors or Gray code. FrameScan is particularly useful for testing connectors or devices where knowledge of the device internals is limited. It requires a bed-of-nails pin contact on the circuit trace of each device lead to be tested.

FrameScan is not effective for testing devices lacking mechanical access, or devices with heatsinks.

The flowchart below may help determine if FrameScan is appropriate for testing a particular device.



FrameScan Requirements

Before you can create a FrameScan test, you must define continuity groups and the FrameScan reference node.

Continuity Groups

Define continuity and jumper tests either in the input list or by building a continuity or jumper component test. For FrameScan tests, continuity group definitions are required before you run Generate. PGEN also needs a power statement indicating VCC/GND nodes to identify the pin types Power and Ground.

During a FrameScan test, the tester connects all nodes to ground except the MultiScan reference node, the node being tested, and any nodes connected to the node being tested. FrameScan uses information in the Interconnect section to identify nodes that connect to the node being tested.

MultiScan Reference Node

Establish a MultiScan Reference node if one does not already exist. The transceiver uses the reference node to cancel noise from the signal.

The reference node is stored in the Header/PRGMVARS step in the MultiScan Reference Node field. It should appear in the MultiScan Reference Node field, not in the list of Ground Reference Nodes. The reference node default is 9999.

The reference node default in the PGEN.CFG file is 9999. You can specify the reference node by editing Header/PRGMVARS or PGEN.CFG file, as explained in “Set Up PGEN.CFG” on page 3-8.

Selecting a Reference Node

The reference node must be an unused node. It occupies a single tester node. You must define a single reference node to be used for all FrameScan tests. The reference node must connect to the ground bus of the board under test. The node you enter must be the same node as is wired in the fixture. Although you can use any valid unused tester node number as the reference node, we recommend that reference nodes be chosen from available Sense nodes. If the program uses the G-pole for power-supply grounding, the reference nodes must be chosen from available Sense nodes.

The reference node must be in a different 16-node group from the device ground and from any power supply. For example, if you have a device ground at node 0, put the MultiScan Reference at node 16. Do not use the system ground node 0 as the reference node. Use node 16 when possible.

Checking Reference Node Wiring

You may need to verify that the reference node is wired correctly (for example, if device test failures are intermittent). For this test, Teradyne recommends that you choose an available sense node from the fixture interface. This means that the node is in the upper 16 node group of the D/R board. Any power supplies connected to the same 16 node group on any D/R board cannot use G-Pole shorting for grounding.

The fixture probe that contacts the board ground should have only a single wire on it. The wire connects the DUT board ground to a node in the tester. A common error in wiring the reference node is the addition of wires to the fixture ground plane, V reeds, or DUT power supply. Record the reference node you have established for later use during program generation. This reference senses ground at the board under test. Establishing the proper reference node is mandatory for dependable FrameScan results.

FrameScan PRGMVARS

Header/PRGMVARS includes the following General and Report Variables important to FrameScan testing. If you use FrameScan, check these variables.

For a description of all fields in Header/PRGMVARS, refer to the **Z1800-Series Programmer's Guidebook**.

```
18xx Windows mode-init_com
Edit   Save   Revert   Quit
                                   Header                                  [ ↓ ]-[ ↓ ]
( √ )  General Variables   (  )  Report Variables
                              General Variables
Vacuum Select            : Vacuum 1      Vacuum Delay (mS)        : 100
Auto Probe Check (APC):  Off             Stop On Fail (SOF)       : Off
Digital HiCheck          : Off           Skip On Fail             : Off
Digital Tracer           : Off           Backdrive Timeout (mS)   : 0.0
Section Abort            : On            Duty Cycle (%)           : 0
Abort On Fail Count      : 0             Learn Cap Phase Offsets  : Off
Discharge Method         : DschrgSect    DR1 Emulation            : Off
MultiScan Discharge      : On            DFP Configuration        : Off
Power Down Sequence      : Reverse       External Power Down      : Off
Ground Reference Nodes  (      ) (     ) (     ) (     ) (     )
MultiScan Reference Node ( 340)   FrameScan Plus Measure (99)
DeltaScan, Short Pwr/Gnd via G-pole:   Off
DeltaScan, Verify Pwr/Gnd Shorting:    Off
DeltaScan, Fixed Threshold:            50

Board Description        [                                                ]
Dscan retry              [5 ]        Dscan retry delay          [  1] ms
Dscan Run ALL Pin Pairs  On          Dscan Hard Fixed Thresh  [Off]
Dscan will run all posible pin pairs for data collection
C:/TPD/DEMO\DEMO_172 - ICT     START     CANCEL     SOF   HLD   RPT   CRT
```

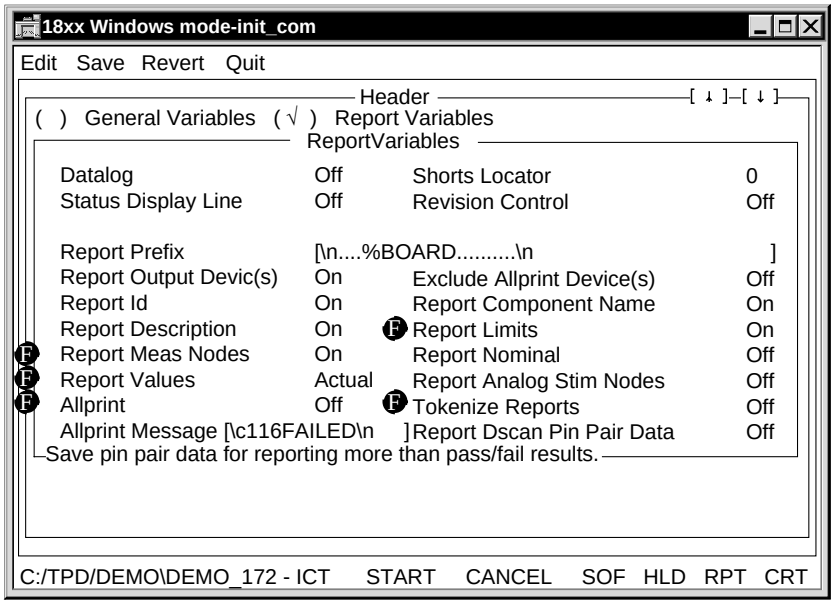
FrameScan variable

General Variable

- **MultiScan Reference Node**

  Senses the actual ground level of the board under test.

Note: The default MultiScan Reference node in the PGEN.CFG file is 9999. You can specify the reference node by editing the PGEN.CFG file before generation or entering the reference node in Header/PRGMVARS at any time.



F **FrameScan variables**

Report Variables

- **Report Meas Nodes**

  Off: The pin number is included in the report, but the node number is not included.

  On: The node number is included after the pin number in the report. The report includes one line per failing pin.

- **Report Values**

  Off: The report does not include any of the measured values.

  Actual: The report includes the actual measured values.

  Percent: If you select percent, the report includes actual values, since FrameScan tests do not report percent.

  If Report Values is Actual or Percent the report includes one line per failing pin.

- **Report Limits**

  On: The report includes the Pass/Fail limits of the test.

- **Allprint**

  On: A report is generated for every test, not just the failing tests.

- **Tokenize Reports**

  On: The Datalog and CRT reports are in Tokenlog format. The report file is TOKENLOG.DAT and is in the TPD\PROGRAM directory.

Developing FrameScan Tests

This section explains how to add FrameScan tests to a new board test program.

- **To develop FrameScan tests:**

  1. Set up FSCAN tokens.
  2. Update the PGEN.CFG file.
  3. Generate tests.
  4. Validate and troubleshoot tests.

Adding to an existing board test program To add a FrameScan test to an existing board test program, follow the procedures outlined in the **Z1800-Series Programmer's Guidebook** for incremental test generation.

Note: If board topology has changed, run PGEN/Learn to reestablish the continuities, special cases, shorts, and merged special cases on the board.

Set Up FSCAN Tokens

The Input List (IPL) is an ASCII file that contains a complete description of the board component parts and interconnections. For a FrameScan test, modify the IPL syntax by adding an IPL record to support the FrameScan test type.

IPL Record

A record is a section of the input list file IPL.DAT dedicated to a single component test step. Like all other component tests, a FrameScan test is governed by its input list record.

Record for a FrameScan test:

Token	ID	Description	Name	X Inducer	Node List
FSCAN,	P1_A,	"FrameScan Test",	P1,	X17,	3,17,16,15,14

Major and Minor ID Follow the Major/Minor ID convention for all components tested with both FrameScan and other tests methods.

- The major ID is the part of the ID that comes before a dash or hyphen (-) or an underscore (_).
- The minor ID is any part after the major ID, including the dash or underscore.

In P1_A, for example, P1 is the major ID and _A is the minor ID.

Add a unique minor device ID to each new component entry. For example, use _FS, so that P1 becomes P1_FS. The major device ID, P1, will not be in conflict with P1_FS.

Inducer Number The inducer number specifies which inducer to use for the component to be tested. You must type an x in front of the inducer number to distinguish the inducer number from the list of node numbers.

Node List First node in the list is the first pin on the device, second node is the second pin, and so on for each pin on the device up to 625 pins. Use the number 9999 for an unconnected pin.

Refer to the **Z1800-Series Programmer's Guidebook**, Chapter 7, "Program Generator Tools," for more information about record syntax in general.

Set Up PGEN.CFG

Settings in the PGEN.CFG file configure the program generate function. You can edit the PGEN.CFG file to specify other FrameScan test default values for PGEN instead of the standard defaults.

For a complete discussion on editing the PGEN.CFG file, refer to the **Z1800-Series Programmer's Guidebook**, Chapter 7, "Program Generator Tools."

The following fields in the PGEN.CFG file apply to FrameScan:

- **MSCANREF**

  MultiScan reference node is an otherwise unused node that specifies the reference node for a FrameScan test. The MultiScan reference node is stored in the Header/PRGMVARS worksheet of the test program for the board.

  Although the default is 9999, the value should be set to a valid reference node. You can specify the reference node by editing the PGEN.CFG file before generation or entering the reference node in Header/PRGMVARS at any time.

  PGEN adds this node to the Header/PRGMVARS Multiscan reference node field during incremental program generation.

- **WSCANTHRESH**

  WaveScan Measurement Threshold specifies a measurement threshold in tenths of a microvolt. The program generator uses this value in generating a FrameScan test. For a pin to be detected, the measured value must be higher than the threshold.

  Values may be from 1 to 32,000. The default is 100 (10µV).

Build the Database File

Once edits are completed, save the IPL, and continue with these steps:

- **To build a new board test:**

  1. Run **PGEN/CLEAN**.
  2. Run **PGEN/BUILD.**

     This command creates a new temporary IPL database, IPL.DBF.

- **To build an existing board test:**

  Do NOT run PGEN/CLEAN. Run **PGEN/BUILD**.

  If you accidentally select PGEN/CLEAN, copy the board directory from your backup and start over.

Generate Tests

The PGEN/Generate command automatically generates the test program ICT.TST from the IPL. The process for developing and executing a test program that uses FrameScan is the same as the existing processes for developing a Z1800-Series test program.

The three test generation methods are automatic program generation, incremental program generation, and manual program generation. They are described in the **Z1800-Series Board Test Tutorial**.

Important: The Programmer Efficiency Package (PEP) does not recognize FrameScan tokens and will not perform an analysis on them in the input list.

- **To automatically generate a test:**

  1. Run **PGEN/GENERATE**.

     This command adds the IPL.DBF entries to the main test program ICT.TST. Do not be concerned about messages regarding missing power or ground. Updating and subsequently running Validate eliminates such messages.

2. Run **PGEN/UPDAT**E.

   This command is needed to finalize topology for all reports and before any Validates. The update is critical for success.

3. After generating FrameScan tests, review the resulting worksheets.

   Make sure that the Multi-Scan Reference node, thresholds, nodes, etc. have been set correctly:

Validating and Troubleshooting Tests

Use PGEN/VALIDATE and your own analysis of system worksheets and reports to achieve maximum test coverage and eliminate false passes, false fails, and unstable tests.

The Validate process puts test steps through an automatic analysis process. In addition, the FrameScan worksheets, Topology and Board Fault Coverage reports, and FrameScan database all provide information for troubleshooting tests.

Make edits to the worksheets and the database, as needed, to improve the tests. Follow this process:

- First, look at the Topology report for component node and ID problems. Edit the test program ICT.TST before you run Validate.
- Validate the tests.
- Look at the FrameScan worksheets, Board Fault Coverage report and FrameScan database. Modify or add pin-pairs, threshold values, etc. in the database or worksheets.
- Continue to run Validate and edit component and test attributes until you have the program perfected.

This section covers validating and troubleshooting suggestions, tools and processes. For complete information, also read Chapter 7, “Program Generator Tools” and Chapter 9, “Test and Debug Tools” in the **Z1800-Series Programmer’s Guidebook**.

Validate Tests

The Validate tool provides a way to learn test parameters from a known good board. Validate is required for FrameScan test development because the default thresholds may result in some false failures. Validate is necessary to help select the correct threshold for the conditions on the board.

- **To validate FrameScan test programs:**

1. Select **Validate** from the Setup menu.

   The system displays the Validate Configuration window.

2. Select **Validate FrameScan**.

3. In the **Threshold Variance Reported** field, specify the variation in tenths of microvolts the system uses to determine whether it will write a message into the EXCEPT.LST file when Validate changes the measurement threshold in a FrameScan test.

   If Validate determines that the proper measurement threshold varies from the test page default value by a value that is greater than the test page default, it writes a message into the EXCEPT.LST file. It does not write a message if the variance is less than the default value.

   The range of acceptable values is 0 to 255.

4. In the **Minimum Threshold Allowed** field, specify the minimum threshold Validate sets before changing a pin to Not Tested.

   For FrameScan, the default is 30. The range is 30 to 32000.

5. Run **Validate** from the FrameScan section or FrameScan component editor using a known good board on the fixture.

   Prior to making any measurements, Validate runs the same calibration routine that is run when a test begins.

   If Validate is unable to achieve signal level high enough to allow a reasonable threshold, it changes the pin from Normal to Not Tested in the worksheet. If Validate finds a significant portion of the signal is noise or crosstalk, it also changes the pin to Not Tested.

   Validate generates a report listing each parameter it changed. The report goes to the exception list file, EXCEPT.LST. You can filter inconsequential changes from the report using **Setup/Validate/Validate FrameScan/Threshold Variance Reported**.

Note: If you are not sure of the quality of the available supply of boards used for Validate, you need to examine each FrameScan test, determine the cause of problems, correct them if possible, then re-validate.

6. Run **Validate** on additional good boards.
7. Troubleshoot any failures.

   See the troubleshooting suggestions in the topics below.
8. Revalidate individual devices as necessary to get repeatable and stable tests on the sample boards.

MultiScan Failure Flag A system flag called MultiScan Failure is set if any MultiScan test fails, including FrameScan. If the Section Abort feature is enabled, a failure causes the software to jump to the Trailer.

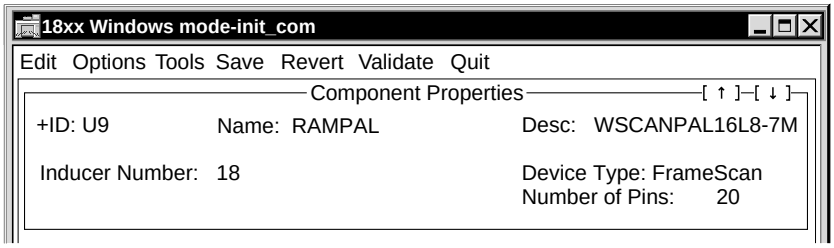
Troubleshoot Tests

This section contains suggestions for making test program corrections. Start troubleshooting by examining the test worksheets and reports.

Edit FrameScan Worksheets

Use the fields and controls of the FrameScan worksheets to troubleshoot tests.

Component Identifier Section The FrameScan Component Identifier section specifies the information required to generate a FrameScan test for a component. You can provide the information either by invoking Build on the input list or by invoking Edit to add a FrameScan component and using the editor to fill in the information.



Component Identifier Fields:

- **ID**

  The ID field is the component identifier, for example U9.
- **Name**

  The name field contains the device name.

- **Desc**

  The description field contains a text description of the test, for example, “FrameScan test for U9.”

- **Device Type**

  This field can contain WaveScan, FrameScan, or FrameScan Plus; select FrameScan to create a FrameScan test.

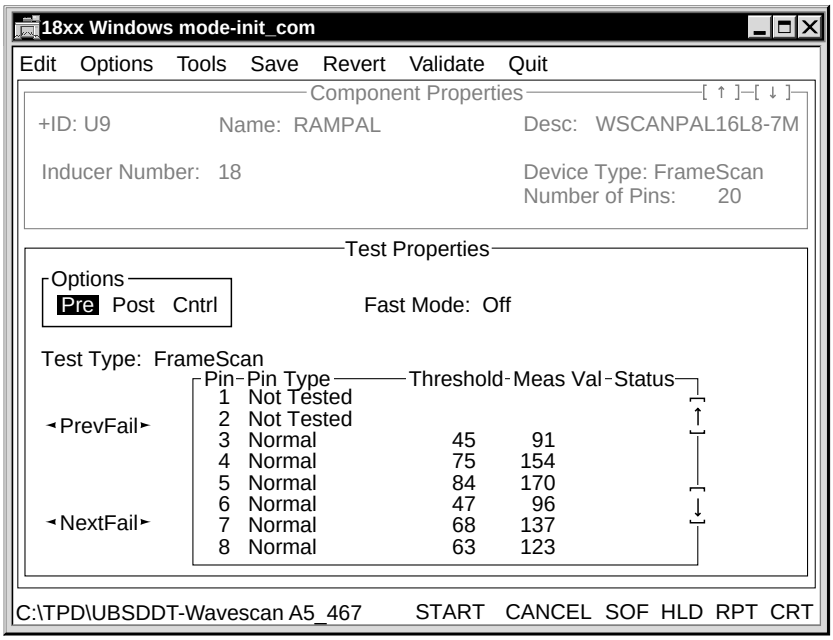
- **Number of Pins**

  Use this field to specify the number of pins (1 to 625) on the device to be tested. Click on this field to open to the Node Entry dialog box. Enter only one node number for each device pin.

- **Inducer Number**

  Enter an integer from 1 to 255 to indicate which inducer to use to stimulate the component being tested.

Test Properties Section The Test Properties section of a FrameScan worksheet displays test parameters and results. From here you edit and execute the test step.



Test Properties Fields:

- **Options Box**

  The Options box contains three selections, Pre, Post, and Cntrl, each of which causes a pop-up window to appear. The pop-up windows appear when you select Options from the menu bar, then select Pre-Test Options, Post-Test Options, or Controls from the pulldown menu.

  Because the Z1800-Series system software does not regain control between FrameScan tests, relays and external programs are not available in the FrameScan worksheet pre- and post-test options.

- **Test Type**

  The test type can be FrameScan or WaveScan. The Z1800 software generates the type specified by the Device Type entry in the component identifier portion.

- **Fast Mode**

  You can turn Fast Mode testing On or Off with this field. Fast Mode can be used in situations where test speed is important and testability is already proven.

Note: Fast Mode removes noise measurement and signal averaging from the test result, so its results may not be as stable as Normal Mode (Fast Mode Off) results.

- **FrameScan Pin Parameter Window**

  FrameScan's Pin Parameter window allows you to specify the test parameters for each pin. You may specify the pin type and measurement threshold. FrameScan software fills in the measured value and test status fields after the test is run.

  The Pin Parameter default values are:

  - Pin Type—Normal
  - Measurement Threshold—100.

  The screen reflects the system resolution of approximately one-tenth of a microvolt (0.1 µV). For example, a threshold of about 20 µV appears as a value of 200.

  You may enter information for up to 625 pins in the Pin Parameter window. Use the scrolling arrows at the right edge of the screen or the keyboard's arrow keys to move through the screen.

  The Prev Fail (previous) and Next Fail buttons at the left edge of the screen scroll the display to the previous or next failing pin.

- **Pin Type**
  - Normal. The pin is an independent signal pin.
  - Normal Tied. For each tied group of pins, one pin has the Normal Tied pin type and all others have the Tied pin type. The tester measures a Normal Tied pin in the same way it measures a Normal pin. The Normal Tied pin fails when all pins tied to the same node are open. If some of the tied pins are connected, the test may or may not fail. In FrameScan tests, the measured signal is usually directly proportional to the number of pins tied together.
  - Tied. The pin is tied to another device signal pin. No test is made for pins marked Tied. In a group of pins connected to the same node, one pin is marked Normal Tied. FrameScan test results are reported for this pin only, although the test results could indicate any or all pins in the Tied group. See the description for Normal Tied.
  - Ground. The pin is either a ground pin for the device or a signal pin tied to ground.
  - Power. The pin is either a power pin for the device or a signal pin tied to a power voltage.
  - N/C (Not Connected). The pin is either not connected inside the device package or is not connected to a nodal pin.
  - Not Tested. The pin is not to be tested. Validate changes pins from Normal to Not Tested when it cannot make a reliable measurement. Once a pin is marked Not Tested, Validate does not attempt to make a test for the pin.

- **Threshold**

  The threshold is the minimum level of signal that indicates the presence of an induced signal rather than random system noise. To avoid cross-talk, the threshold is set higher if the received signal is higher.

  The measurement threshold field specifies the AC voltage used to determine whether a pin passes or fails the FrameScan test. If the measured voltage is below the threshold, the pin is determined to be open. If the measured voltage is equal to or above the threshold, there is no open on that pin.

  The threshold range is 1 to 32,000.

Because Validate determines the optimum threshold values to use for a FrameScan test, usually you need not change any settings. However, if you would like to use a value other than that set by Validate, you may do so. You may type the new values into the worksheet after you have run Validate. You can change the default value using the WSCANTHRESH parameter in the PGEN.CFG file.

Threshold is relevant only for Normal and Normal Tied pins. This field is blank for other pin types.

- **Meas Val**

  This field shows the actual measured voltage of the pin in tenths of a microvolt.

- **Status**

  The Status field indicates whether the pin passed or failed the test. This field is blank unless the pin fails.

- **Prev Fail and Next Fail**

  Use the Prev Fail ("previous fail") and Next Fail buttons to move from the current pin to the previous or next failing pin. After each burst, Prev Fail and Next Fail are referenced from Pin 1 of the device.

  Select the buttons by either clicking with the mouse or positioning the cursor on the button and pressing Enter. While you are in the pin parameter window, you can use the key combinations of Ctrl-Up Arrow to move to Prev Fail and Ctrl-Down Arrow to move to Next Fail.

Interpreting Measured Values When testing takes place, the receiver sensitivity is adjusted at each pin measurement so that the threshold is in the middle of the receiver's dynamic range.

- **9999—Good**

  If the measured signal is above the threshold and above the receiver limit, the worksheet displays the number 9999 instead of a measurement value and the pin passes. Passing is the correct conclusion, since a limiting signal is certain to be above the threshold.

  9999 readings indicate a large measured signal. If measured results change from a "real" value to 9999, it means the measured signal is near limits. 9999 signals are good.

  - To know what the level actually is on that pin, raise the threshold temporarily and repeat the test. The measurement will be repeated at a lower sensitivity.
  - To avoid false failures, keep the thresholds that Validate selected. These thresholds may result in the receiver reaching limits for many pins, and the Meas Val field displaying 9999.

- **8888—Bad**

  An 8888 result in the Meas Val field indicates that a large amount of noise is present for that pin. An 8888 display indicates a problem.

  The noise may be caused by the demultiplexer board being located too close to fixture wiring, producing too much crosstalk.

  - To correct crosstalk, place the demutiplexer board outside the fixture pan as far away from fixture wiring as possible. If you continue to receive 8888 readings, use shielded cable to connect to the demultiplexer board and shield the demultiplexer board inside a Mu metal box.
  - If the Meas Val field continues to display 8888 after shielding, change the pins reporting 8888 to Not Tested. Validate changes pins that have too much noise to Not Tested.

Review FrameScan Output

FrameScan output includes Statistics reports, Datalog CRT reports, and Tokenlog reports.

FrameScan Statistics Report The FrameScan Statistics (Fault Coverage) report indicates the fault coverage for the device-under-test (DUT). The fault coverage is a percentage: the number of tested pins divided by the number of pins included in the FrameScan fault coverage analysis. The number of pins included in the FrameScan fault coverage analysis is not necessarily the number of pins on the device.

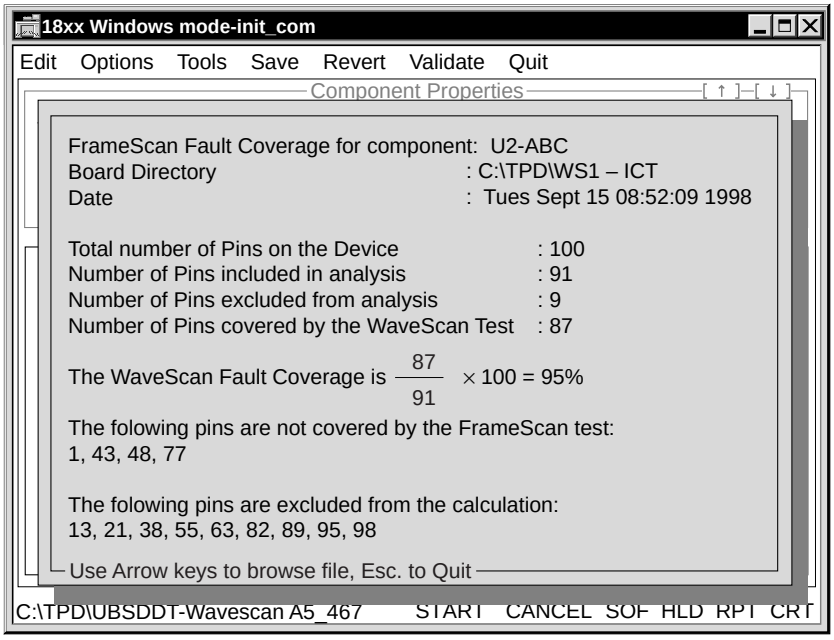
The FrameScan Statistics report lists the pins covered by the FrameScan test and the pins excluded from the calculation. The Statistics report treats the pin types as follows:

Fault Coverage Contents	Pin Types
Pins covered and included in the analysis:	Normal
	Normal Tied
Pins not covered but included in the analysis:	Tied
Pins not covered or included in the analysis:	Ground
	Power
	Not Connected (N/C)
	Not Tested

- **To view the Statistics report:**

1. From FrameScan worksheet menu bar, select Tools.
2. From the pulldown menu, select Statistics.

   A window appears as illustrated.



3. Select **Esc** to quit the report display.
4. Save the Statistics report to a file. The file name has the extension .TXT.

FrameScan Datalog/CRT Reports When you execute a FrameScan test, the software generates a report. If Allprint is On, the report includes both passing and failing test results. If Allprint is Off, the report is limited to failing tests.

FrameScan Tokenlog Reports FrameScan test results will be logged by Tokenlog if you select Tokenlog in the Setup-Data-Program Execute channels window. If you select Tokenize Reports from PRGMVARS in the Header, the Datalog and CRT reports will be in Tokenlog format. The report file is TOKENLOG.DAT and is in the TPD\PROGRAM directory.

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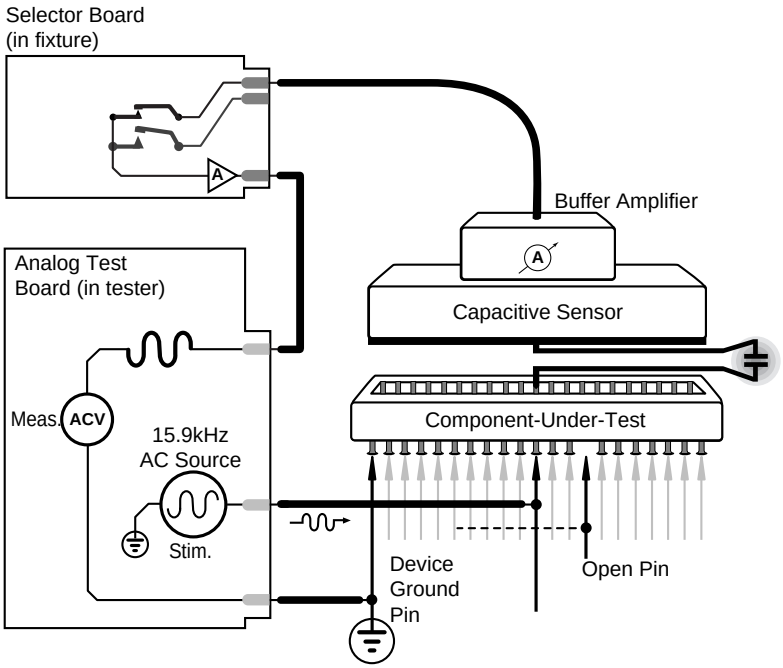
CHAPTER 4 FRAMESCAN PLUS

FrameScan Plus uses capacitive coupling to test device connections on circuit boards. A stimulus signal is applied to the device-under-test (DUT). A sensor above the DUT sends the resulting signal back to the tester, verifying proper connection or locating bad connections.

Theory of Operation

FrameScan Plus employs the phenomenon of capacitive coupling. It sends a stimulus signal from the Analog Test Board (ATB) through the bed-of-nails to the pin of the device under test. A sensor mounted directly above the device capacitively couples the signal through a buffer amplifier, then through the selector board back to the ATB for measurement.

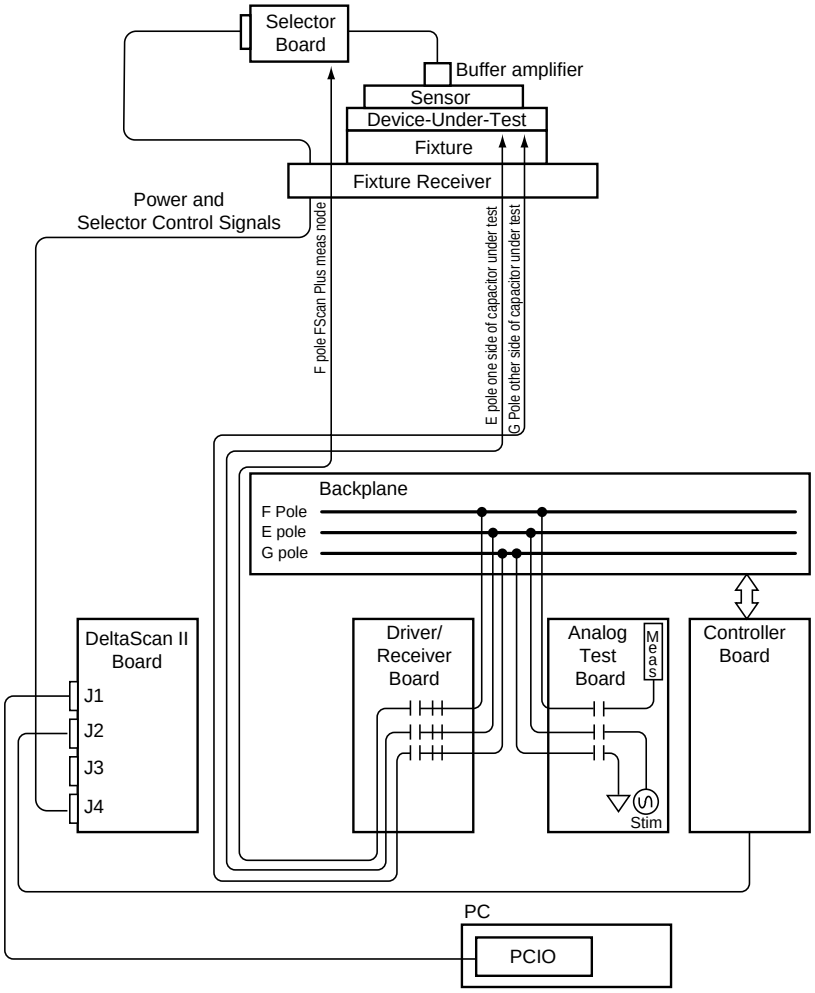


FrameScan Plus Hardware

FrameScan Plus uses the Analog Test Board (ATB), which is the standard Z1800-Series instrument for stimulus and measurement. Additional hardware requirements for FrameScan Plus consist of:

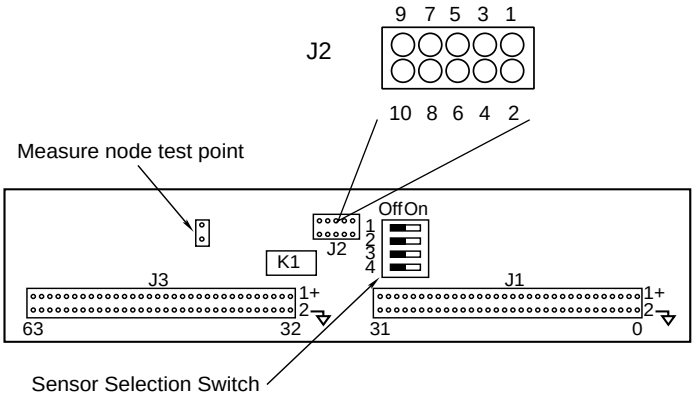
- Fixture-mounted selector board for selecting the sensors
- FrameScan Plus sensor/buffer board over each device to be tested
- DeltaScan II board and cable for powering and controlling the selector board

Information on specific fixture wiring can be found in the **Z1800-Series Fixturing Guidebook**.



Selector Board

The selector board (PN 051-065-00) is the part of the fixture that enables the sensor so it can detect an AC signal and routes the selected sensor output to the measurement node.



Inside the tester, a cable routes the power and control signals from the DeltaScan II board to the fixture receiver. The signals pass via transfer pins through individual wires to a ten-pin jack, and through a ten-pin ribbon cable to J2 on the selector board.

Sensor Selection Switch States

Each selector board can accommodate up to 64 sensors and can be chained to additional selector boards up to a maximum of 1024 sensors.

Sensor groups are selected or deselected by address according to the position of the Sensor Selection Switch DIP, as shown at the right.

Sensor Group	Switch State: 4	3	2	1
0-63	Off	Off	Off	Off
64-127	Off	Off	Off	On
128-191	Off	Off	On	Off
192-255	Off	Off	On	On
256-319	Off	On	Off	Off
320-383	Off	On	Off	On
384-447	Off	On	On	Off
448-511	Off	On	On	On
512-575	On	Off	Off	Off
576-639	On	Off	Off	On
640-703	On	Off	On	Off
704-767	On	Off	On	On
768-831	On	On	Off	Off
832-895	On	On	Off	On
896-959	On	On	On	Off
960-1023	On	On	On	On

Selector Board Power and Control Wiring

The wiring path should be as follows: Z18xx fixture receiver pins to fixture pan TA row to transfer pins to ribbon cable to J2 pins on the Selector board.

The following illustration shows the fixture TA row pins to be wired to the selector board J2 pins. This information is also available in the **Z1800-Series Fixturing Guidebook**.

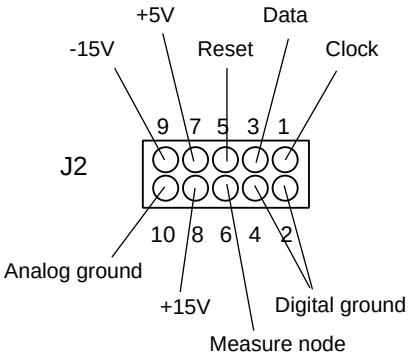
The selector board wiring from the fixture interface (row TA) to the fixture transfer pins must be correct. Individually check each fixture pin listed below with an ohmmeter.

WARNING! Be sure to remove the fixture from the tester interface before the wiring check because +15, - 15, +5, GND may be present at the interface.

Fixture TA Row Pins

```
     |0  22|
     |     |
     |     |
     |   25|
     |     |
     |5    |
+15V |6  28|DATA
     |7  29|RESET
-15V |8  30|CLOCK
     |     |
     |10   |
     |     |
     |     |
     |   35|
     |     |
     |15   |
 +5V |16 39|GND [Analog and
     |     |       Digital]
     |   40|
     |     |
     |21 42|
```

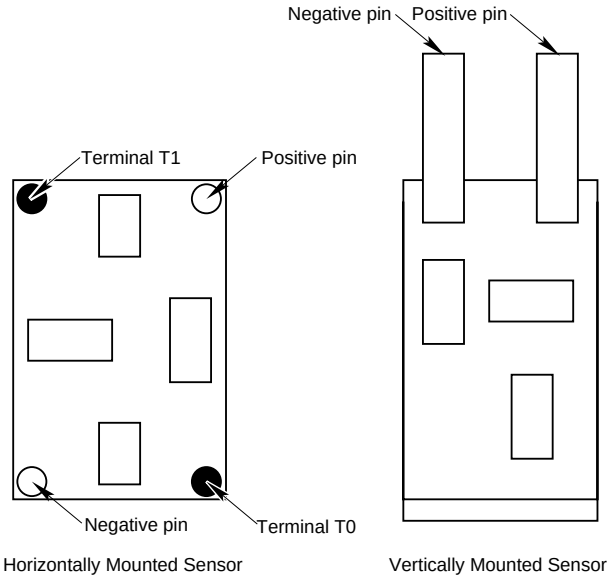
J2 Pins on Selector Board



Sensors

FrameScan Plus sensors can be mounted horizontal or vertical. The sensors are mounted in the fixture above the devices targeted for test on the board under test. The sensors may be attached to an overclamp or they may be in the probe plate beneath the DUT (device under test).

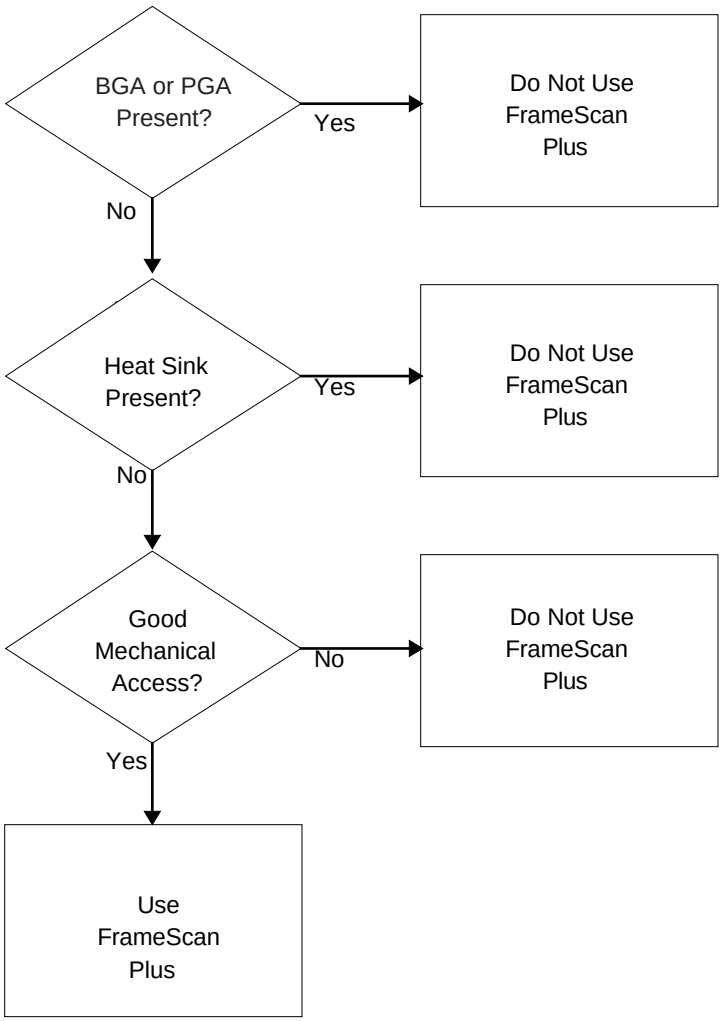
- The horizontal sensor plate is composed of two physically separate plates: a metal ground plate and a metal signal plate. The signal plate is closest to the DUT.
- The vertical sensor plate is a single metal plate.



When to Use FrameScan Plus

FrameScan Plus is a technique that detects proper pin contact in devices. It requires a bed-of-nails pin contact on the circuit trace of each device lead to be tested.

The flowchart below may help determine if FrameScan Plus is appropriate for testing a particular device.



FrameScan Plus Requirements

Before you can run Validate on a FrameScan Plus test, you must adjust fixture wiring and define continuity groups and the FrameScan Plus measurement node.

Fixture Wiring

To set up for a FrameScan Plus test, wire the fixture so that the V-pins connect to the ground of the board under test as you would when wiring for a digital test, even if no power-on tests will be done.

Continuity Groups

Define continuity and jumper tests either in the input list or by building a continuity or jumper component test. For FrameScan Plus tests, continuity group definitions are required before you run Generate. During a FrameScan Plus test, the tester connects all nodes to ground except the MultiScan Reference Node, the node being tested, and any nodes connected to the node being tested. FrameScan Plus uses information in the Interconnect section to identify nodes that connect to the node being tested.

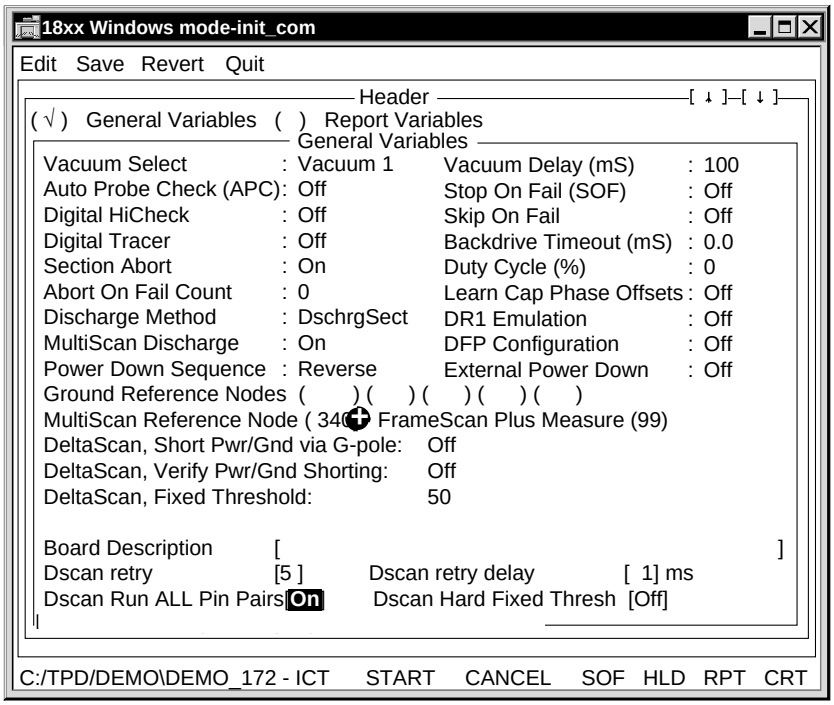
FrameScan Plus Measurement Node

The FrameScan Plus Measurement node is stored in the Header/PRGMVARS/FrameScan Plus Measure Node entry. It must be an otherwise unused node in the tester connecting to the selector board output. During FrameScan Plus tests, the FSPLUS measurement node is switched to the F-pole.

FrameScan Plus PRGMVARS

Header/PRGMVARS includes the following General and Report variables specific to FrameScan Plus testing. If you use FrameScan Plus, set these variables.

For a description of all fields in Header/PRGMVARS, refer to the **Z1800-Series Programmer's Guidebook**.



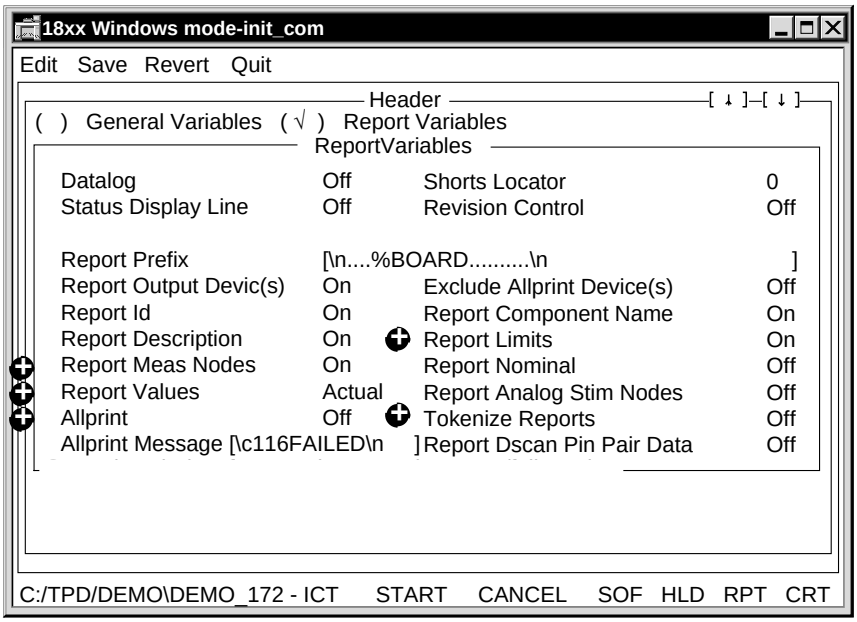
FrameScan Plus variable

General Variables

- **FrameScan Plus Measure**

  The FrameScan Plus Measure node is an otherwise unused node that lets you specify the measure node for FrameScan Plus and CapScan tests. The node is stored in the Header/PRGMVARS worksheet of the test program for the board. The default is 9999.

This is the node that is hardwired to the output of the FrameScan Plus selector board. During a test, the FrameScan Plus Measure node is switched to the F pole.



FrameScan Plus variables

Report Variables

- **Report Meas Nodes**

  Off: The pin number is included in the report, but the node number is not included.

  On: The node number is included after the pin number in the report. The report includes one line per failing pin.

- **Report Values**

  Off: The report does not include any of the measured values.

  Actual: The report includes the actual measured values.

  Percent: If you select percent, the report includes actual values, since FrameScan Plus tests do not report percent.

  If Report Values is Actual or Percent the report includes one line per failing pin.

- **Report Limits**

  On: The report includes the Pass/Fail limits of the test.

- **Allprint**

  On: A report is generated for every test, not just the failing tests.

- **Tokenize Reports**

  On: The Datalog and CRT reports are in Tokenlog format. The report file is TOKENLOG.DAT and is in the TPD\PROGRAM directory.

Developing FrameScan Plus Tests

This section of the chapter discusses how to develop FrameScan Plus tests.

- **To develop FrameScan Plus tests:**

1. Set up FSPLUS tokens.
2. Build the necessary database files.
3. Generate the test.
4. Validate and troubleshoot the test.

Set Up FSPLUS Tokens

The input list (IPL) is an ASCII file that contains a complete description of the board component parts and interconnections. For each FrameScan test, modify the IPL syntax by adding an IPL record to support the FrameScan test type.

IPL Record

A record is a section of the input list file IPL.DAT dedicated to a single component test step. Like all other component tests, a FrameScan test is governed by its input list record.

Token	ID	Description	Name	X Sensor	Node List
FSPLUS,	P1_A,	“FrameScanPlus Test”,	P1,	X17,	3,17,16,15,14

Sensor Number The sensor number specifies which sensor to use for the component to be tested. You must type an x in front of the sensor number to distinguish the sensor number from the list of node numbers.

Node List First node in the list is the first pin on the device, second node is the second pin, and so on for each pin on the device up to 625 pins. Use the number 9999 for an unconnected pin.

Refer to the **Z1800-Series Programmer’s Guidebook**, Chapter 7, “Program Generator Tools,” for more information about record syntax in general.

Major and Minor ID Follow the Major/Minor ID convention for all components tested with both FrameScan and other tests methods.

- The major ID is the part of the ID that comes before a dash or hyphen (-) or an underscore (_).
- The minor ID is any part after the major ID, including the dash or underscore.

In P1_A, for example, P1 is the major ID and _A is the minor ID. Add a unique minor device ID to each new component entry. For example, use _FS, so that P1 becomes P1_FS. The major device ID, P1, will not be in conflict with P1_FS.

Add Power and Ground Nodes

If the power and ground nodes have not been defined, you should build a power test to define them, then run UPDATE before you run GENERATE. If you do not wish to execute the power test, you may disable it.

PGEN also needs a power statement indicating VCC/GND nodes to identify the pin types Power and Ground.

1. Add a power test if necessary.

   If any of the device nodes are connected to other nodes via low impedance paths and have not been added to the appropriate interconnect group, you should add these nodes to the appropriate interconnect group now.

2. Add interconnects if necessary.

Update PGEN.CFG

Settings in the PGEN.CFG file configure the program generate function. You can edit the PGEN.CFG file to specify other FrameScan Plus test default values for PGEN to use instead of the standard defaults. For a complete discussion on editing the PGEN.CFG file, refer to the **Z1800-Series Programmer's Guidebook** Chapter 7, "Program Generator Tools."

The following field in the PGEN.CFG file applies to FrameScan Plus:

- **FSPMEAS**

  The FrameScan Plus Measure node is an otherwise unused node that lets you specify the measure node for FrameScan Plus and CapScan tests. The node is stored in the Header/PRGMVARS worksheet of the test program for the board. The default is 9999. This is the node that is hardwired to the output of the FrameScan Plus selector board.

Build the Database File

Once edits are completed, save the IPL, and continue with these steps:

- **To build a new board test:**

  1. Run **PGEN/CLEAN**.
  2. Run **PGEN/BUILD.**

     This command creates a new temporary IPL database, IPL.DBF.

- **To build an existing board test:**

  Do NOT run PGEN/CLEAN. Run **PGEN/BUILD**.

  If you accidentally select PGEN/CLEAN, copy the board directory from your backup and start over.

Generate Tests

The PGEN/GENERATE command automatically generates the test program ICT.TST from the IPL. The process for developing and executing a test program that uses FrameScan Plus is the same as the existing processes for developing a Z1800-Series test program.

The three test generation methods are automatic program generation, incremental program generation, and manual program generation. They are described in the **Z1800-Series Board Test Tutorial**.

Important: The Programmer Efficiency Package (PEP) does not recognize FrameScan Plus tokens and will not perform an analysis on them in the input list.

- **To automatically generate a test:**

  1. Run **PGEN/GENERATE**.

     This command adds the IPL.DBF entries to the main test program ICT.TST. Do not be concerned about messages regarding missing power or ground. Updating and subsequently running Validate eliminates such messages.
  2. Run **PGEN/UPDATE**.

     This command is needed to finalize topology for all reports and before any Validates. The update is critical for success.
  3. After generating FrameScan Plus tests, review the resulting **worksheets**.

     Make sure that the FrameScan Plus Measurement node, thresholds, nodes, etc. have been set correctly.

Validating and Troubleshooting Tests

The Validate process puts test steps through an automatic analysis process. Use PGEN/VALIDATE and your own analysis of system worksheets and reports to achieve maximum test coverage and eliminate false passes, false fails, and unstable tests.

Follow this process:

- Validate the tests.
- Look at the FrameScan Plus worksheets and the Statistics, Datalog, and Tokenlog reports.
- Check FrameScan Plus hardware.
- Continue to run Validate and edit component and test attributes until you have the program perfected.

Validate Tests

The Validate tool provides a way to learn test parameters from a known good board. Validate is required for FrameScan Plus test development to find threshold values that will give reliable test results.

- **To validate the test program:**

1. Select **Validate** from the Setup menu.

   The system displays the Validate Configuration window.

2. Make sure that the **Validate FrameScan Plus** field is checked.

3. Set the **Minimum Threshold Allowed** field.

   This is the minimum threshold Validate sets before changing a pin to the pin-type Not Tested. For FrameScan Plus, the default is 25; the range is 20 to 32000.

4. Using a known good board on the fixture, run **Validate**.

   Validate processes a FrameScan Plus test step in the same way whether you run Validate for the entire program, for the current section, or for the individual test step.

   To test a pin of a device, FrameScan Plus connects the E-pole to the node connected to that pin, connects the F-pole to the FrameScan Plus measurement node, and grounds all other nodes except nodes in continuity with the Stim pin. FrameScan Plus also enables the sensor for use in the test, connects the selected sensor's output to FrameScan Plus measure node, and closes the V-reeds on all DR boards to create a solid connection between the ground of the board under test and the tester's ground.

   If Validate is unable to achieve signal level high enough to allow a reasonable threshold, it will change the pin from Normal to Not Tested in the worksheet.

   Validate generates a report listing each parameter it changed. The report goes to the exception list file, EXCEPT.LST. You can filter inconsequential changes from the report using **Setup/Validate/Validate FrameScan Plus/Threshold Variance Reported**.

5. Troubleshoot any failures.

   FrameScan Plus worksheets and reports provide information for troubleshooting. In addition, check the sensor board, buffer/sensor, and fixture wiring.

6. Revalidate individual devices as necessary to get repeatable and stable tests on the sample boards.

MultiScan Failure Flag The MultiScan failure flag is set if a test fails. If the Section Abort feature is enabled, a MultiScan failure causes a jump to the Trailer at the end of the WaveScan/FrameScan/FrameScanPlus section.

Troubleshoot Tests

This section contains suggestions for making test program corrections. Start troubleshooting by examining the test worksheets and reports.

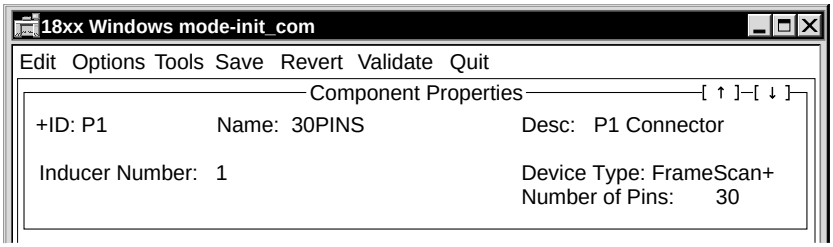
Edit FrameScan Plus Worksheets

The questions below cover FrameScan Plus issues that can be verified or corrected in the test program. If the measured values in the worksheet are near zero, use the following suggestions to troubleshoot the test. Suggestions are listed so that the easiest, least disruptive activities appear first.

- Is the FrameScan Plus Measure Node correct?
- Is each pin node in the worksheet correct?
- Looking at the schematic drawings, does the pin type shown in the worksheet (such as PWR, GND, NORMAL, and so on) correctly match the signal type drawn on the schematic?
- Is the component identifier device type field “FrameScan+”?
- Is the correct sensor number in the worksheet?
  (Locate the sensor over the part; follow the positive pin and negative probe pin wiring to the selector board; observe the position of the wires on the selector board connector J1 OR J3. Sensor numbering starts at with zero. Sensor number 0 is the first physical position on connector J1 of board 1.)

Use the fields and controls of the FrameScan Plus worksheets to troubleshoot tests.

Component Identifier Section The Component Identifier section of a FrameScan Plus worksheet specifies the information required to generate a FrameScan Plus test for a component. You previously set up the information by running Build and Generate on the IPL or manually adding a FrameScan Plus component and filling in the information on the worksheet.



Component Identifier Fields

- **ID**

  The ID field is the component identifier, for example “P1.”
- **Name**

  The name field contains the device name.
- **Desc**

  The description field contains a text description of the test, for example, “FrameScan Plus test for P1.”
- **Device Type**

  This field can contain WaveScan, FrameScan, or FrameScan Plus; select FrameScan Plus to create a FrameScan Plus test.

- **Number of Pins**

  Use the Number of Pins field to specify the number of pins (1 to 625) on the device to be tested and to invoke the Node Entry dialog box. You may enter only one node number for each device pin.

- **Node Entry Before Generating Test**

  The Node Entry box pops up when you click on the number in the Number of Pins field. (Use the node number 9999 to indicate an unconnected pin. As such, 9999 becomes a place holder for the node number location.)

- **Node Entry With Worksheet**

  Each pin marked Normal or Normal Tied must have a legal node number associated with it. The number cannot be 9999.

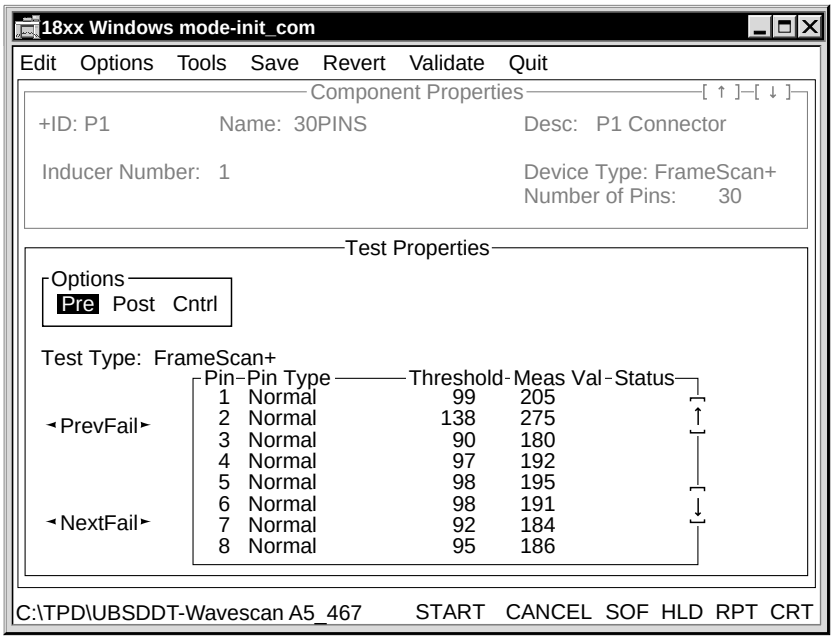
  If you edit nodes **after** you generate the worksheet, you must change any 9999 nodes to N/C (Not Connected). Ideally, the worksheet should be re-generated and run through Validate again if any node numbers have been changed.

  The pin type for an unconnected pin cannot be Normal or Normal Tied.

- **Sensor Number**

  Enter an integer from 0 (zero) to 1023 to indicate which sensor to use to stimulate the component being tested.

Test Properties Section The Test Properties section of a FrameScan Plus worksheet displays test parameters and results. From here you edit and execute the test step.



Test Properties Fields

- **Options**

  Displays the Pre-Test, Post-Test, and Test Page Control options.

- **FrameScan Plus Pin Parameter Window**

  The Pin Parameter window allows you to specify the test parameters for each pin. You may specify the pin type and measurement threshold. The Validate process modifies the measurement threshold, and will change the pin type to Not Tested if the measured signal is below the allowed minimum. FrameScan Plus software fills in the measured value and test status fields after the test is run.

  The Pin Parameter default values are:

  - Pin Type—Normal
  - Measurement Threshold—100.

  The screen reflects the system resolution of approximately one millivolt (1mV). For example, a threshold of about 20mV appears as a value of 20.

  You may enter information for up to 625 pins in the Pin Parameter window. Use the scrolling arrows at the right edge of the screen or the keyboard's arrow keys to move through the screen.

  The Prev Fail (previous) and Next Fail buttons at the left edge of the screen scroll the display to the previous or next failing pin.

- **Pin Type**
  - **Normal**. The pin is an independent signal pin.
  - **Normal Tied**. For each tied group of pins, one pin has the Normal Tied pin type and all others have the Tied pin type. The tester measures a Normal Tied pin in the same way it measures a Normal pin. The Normal Tied pin will fail when all pins tied to the same node are open. If some of the tied pins are connected, the test may or may not fail.
  - **Tied**. The pin is tied to another device signal pin. No test is made for pins marked Tied. In a group of pins connected to the same node, one pin is marked Normal Tied. FrameScan Plus test results are reported for this pin only, although the test results could indicate any or all pins in the Tied group. See the description for Normal Tied.
  - **Ground**. The pin is either a ground pin for the device or a signal pin tied to ground.
  - **Power**. The pin is either a power pin for the device or a signal pin tied to a power voltage.
  - **N/C** (Not Connected). The pin is not connected to a tester node.
  - **Not Tested**. The pin is not to be tested. Validate changes pins from Normal Tied or Normal to Not Tested when it cannot make a reliable measurement. Once a pin is marked Not Tested, Validate will not attempt to make a test for the pin.

- **Threshold**

  The measurement threshold field specifies the AC voltage used to determine whether a pin passes or fails the FrameScan Plus test. If the measured voltage is below the threshold, the pin is determined to be open. If the measured voltage is equal to or above the threshold, the pin is not connected properly. The threshold range is 1 to 32,000.

  Because Validate determines the optimum threshold values to use for a FrameScan Plus test, usually you will not have to change any settings. However, if you would like to use a value other than that set by Validate, you may do so. You may type the new values into the worksheet after you have run Validate. You can change the default value using the WSCANTHRESH parameter in the PGEN.CFG file. Threshold is relevant only for Normal and Normal Tied pins. This field is blank for other pin types.

- **Meas Val**

  This field shows the pin's actual measured voltage in millivolts.

- **Status**

  The Status field indicates whether the pin passed or failed the test. This field is blank unless the pin fails.

- **Prev Fail and Next Fail**

  Use the Prev Fail ("previous fail") and Next Fail buttons to move from the current pin to the previous or next failing pin. After each burst, Prev Fail and Next Fail are referenced from Pin 1 of the device.

  Select the buttons by either clicking with the mouse or positioning the cursor on the button and pressing Enter. While you are in the pin parameter window, you can use the key combinations of Ctrl-Up Arrow to move to Prev Fail and Ctrl-Down Arrow to move to Next Fail.

Review FrameScan Plus Output

FrameScan Plus output includes FrameScan Plus Statistics reports, FrameScan Plus Datalog/CRT reports, and FrameScan Plus Tokenlog reports.

FrameScan Plus Statistics Report FrameScan Plus Statistics (Fault Coverage) report indicates the fault coverage for the device-under-test (DUT). The fault coverage is a percentage: the number of tested pins divided by the number of pins included in the FrameScan Plus fault coverage analysis.

Note: The number of pins included in the FrameScan Plus fault coverage analysis is not necessarily the number of pins on the device.

The FrameScan Plus fault coverage report lists the pins covered by the FrameScan Plus test and the pins excluded from the calculation. The pins excluded from the calculation are Not Connected pins (N/C), Power pins, and Ground pins. The Statistics report treats the pin types as follows:

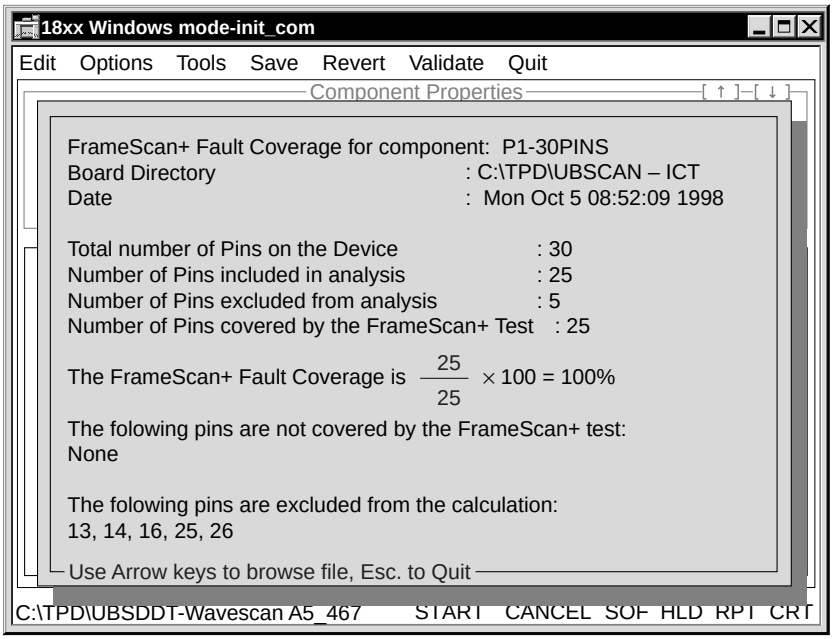
Fault Coverage Contents	Pin Types
Pins covered and included in the analysis:	Normal
	Normal Tied
Pins not covered but included in the analysis:	Tied
Pins not covered or included in the analysis:	Ground
	Power
	Not Connected (N/C)
	Not Tested

- **To view the Statistics report:**

  1. From FrameScan Plus worksheet menu bar, select Tools.
  2. From the pulldown menu, select Statistics.

     A window appears as illustrated.
  3. Select **Esc** to quit the report display.

     A window appears from which you save the Statistics report to a file. The file name has the extension ".TXT" to indicate that it contains ASCII.



FrameScan Plus Datalog/CRT Reports When you execute a FrameScan Plus test, the software generates a report. If Allprint is On, the report includes both passing and failing test results. If Allprint is Off, the report is limited to failing tests.

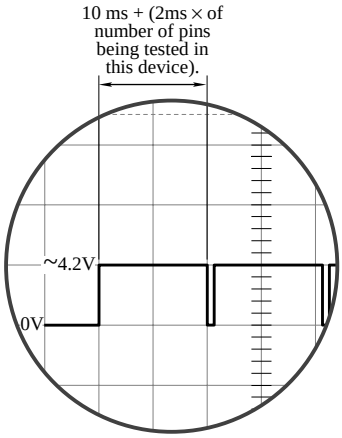
FrameScan Plus Tokenlog Reports FrameScan Plus test results will be logged by Tokenlog if you select Tokenlog in the Setup-Data-Program Execute channels window. If you select Tokenize Reports from PRGMVARS in the Header, the Datalog and CRT reports will be in Tokenlog format. The report file is TOKENLOG.DAT and is in the TPD\PROGRAM directory.

Check the Selector Board

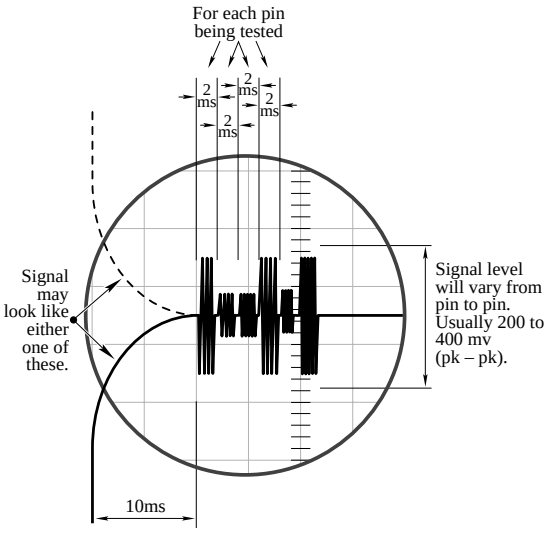
The FrameScan Plus issues below can be verified or corrected on the selector board.

Sensor Selection Switch Make sure that the binary switch on the selector board is set correctly. The switch settings should match the table on page 4-3.

Make sure that the correct sensor is selected by the board. Put worksheet test in Repeat mode. Connect a scope probe on the positive pin of the buffer board. A signal of roughly 4.2 volts should appear on the scope display when the sensor is correctly selected, as illustrated below.

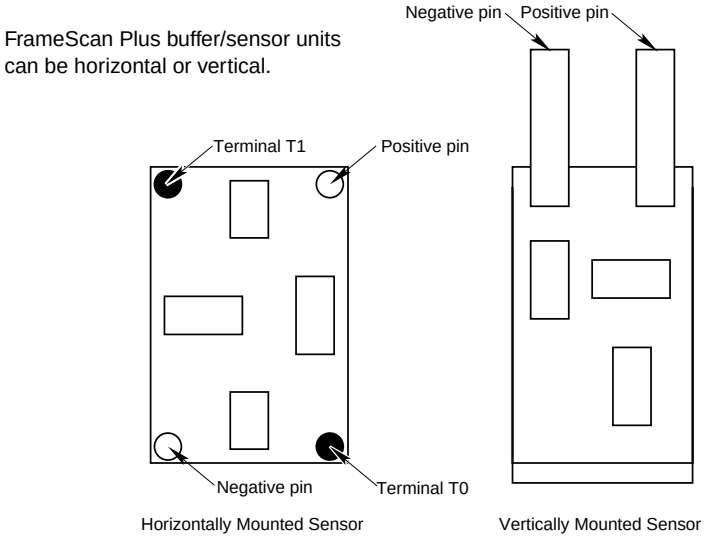


Sensor Board Signal Make sure that the signal from the selector board is as expected. Put worksheet in repeat mode. Connect a scope probe on the selector board test point. When FrameScan Plus is working correctly, the signal on the scope looks like the diagram here.



Check the Buffer/Sensor

Note that the following procedures can be used to test sensors for FrameScan Plus or CapScan tests.



Horizontal Buffer/Sensor With horizontal units, the buffer board should be correctly oriented where it is attached to the sensor plate. It is actually composed of two separate plates: a metal ground plate and a metal signal plate. The signal plate is closest to the DUT.

You can check orientation and functioning two ways: by setting up a trial FrameScan worksheet or by checking connections with an ohmmeter.

Horizontal Buffer/Sensor Worksheet Check To use a trial worksheet to check that the horizontal sensor plate/buffer board:

1. Create a trial **FrameScan Plus worksheet** which has one pin.
2. Assign an unused node to the pin.
3. Assign the sensor number as the sensor under investigation.
4. Connect one end of a clip lead to the unused node you selected, as shown.

   end #1 clip lead end #2
   unused node <----------> use as a probe

5. Bring end #2 of the clip lead near the flat surface of the SIGNAL plate. Make physical but not electrical contact.

   For horizontal buffers, this is the plate closest to the DUT and furthest from the buffer board.

6. Press **Start**. Note the value in the measure field (Value 1).
7. Bring end #2 of the clip lead near the flat surface of the GROUND plate. Make physical but not electrical contact.

   For horizontal buffers, this is the plate furthest from the DUT and closest to the buffer board.

8. Press **Start**. Note the value in the measure field (Value 2).

   If Value 1 is **significantly** greater than Value 2 (for example, if Value 1 is 532 and Value 2 is 14), then FrameScan Plus is functioning correctly.

   Otherwise:

   - Check whether the positive/negative probe wiring is correct.
   - If the positive/negative probe wiring is correct, remove the sensor plate, reverse it, remount it in the buffer plate, then repeat the clip-lead procedures above.

Horizontal Buffer/Sensor Ohmmeter Check You can check the buffer/sensor orientation and connectivity using an ohmmeter. If the setup is correct, you will find:

- Little or no resistance between the exposed Feedthru Hole on the sensor signal plate (the plate closest to the DUT) and T1.
- Large resistance between the exposed Feedthru Hole on the sensor's signal plate (the plate closest to the DUT) and T0.
- Large resistance between T0 and T1.

- **To determine whether the buffer board internal connectivity is correct:**

1. Connect an ohmmeter to T0 and the Negative Probe pin.

   Connectivity is correct when no resistance – zero ohms or 0Ω – appears between T0 and the Negative Probe. Otherwise, the buffer board itself may be defective.

2. Connect an ohmmeter to T1 and the Positive Probe pin.

   Connectivity is correct when a large resistance value appears between T1 and the Positive Probe. Otherwise, the buffer board itself may be defective.

3. Connect an ohmmeter to T1 and T0.

   Connectivity is correct when a large resistance value appears between T0 and T1. Otherwise, the buffer board itself may be defective.

Vertical Buffer/Sensor Check that the sensor plate/buffer board is functioning. The vertical sensor plate is a single metal plate, so there is no possibility of mis-orientation of the sensor plate with respect to the buffer board.

- **To check that a vertical sensor plate/buffer board is functioning:**

1. Create a trial **FrameScan Plus worksheet** which has one pin.
2. Assign an unused node to the pin, then assign the sensor number as the sensor under investigation.
3. Using a clip lead, connect end #1 to the unused node.
4. Bring the other end of the clip lead to the flat surface of the metal plate. Make physical but not electrical contact.
5. Press **Start**.

   A large value should appear in the measure field.

   If a very small value appears in the measure field, check whether the positive/negative probe wiring is correct.

Check Fixture Wiring

Ribbon Cable Check that the cable from the transfer pins to J2 on the selector board is oriented correctly and securely plugged in.

Buffer Circuit Positive/Negative Probe Wiring Selector connectors J1 and J3 are on the bottom side of the selector board. Pins closest to the edge of the board are even numbered pins; pins away from the edge are odd numbered pins. See the FrameScan Plus selector board drawing on page 4-3.

Observe the orientation of the buffer circuit and identify the positive pin and the negative pin. The positive pin should be wired to an odd numbered pin of connector J1 or J3, and the negative pin wired to an even numbered pin of connector J1 or J3.

FrameScan Plus Measure Node Wiring The FrameScan Plus measure node should be wired **only** from an unused node, through transfer pins, to selector board connector J2's pin 6. There should be no other wires connected to the measure node.

Selector Board Power and Control Wiring The wiring path should be as follows: 18xx fixture receiver pins to fixture pan TA row to transfer pins to ribbon cable to J2 pin on selector board.

The selector board wiring from the fixture interface (row TA) to the fixture transfer pins should be correct. Individually check each fixture pin listed in the illustration on page 4-4 with an ohmmeter:

Note: Be sure to remove the fixture from the tester interface before the wiring check because +15, - 15, +5, GND may be present at the interface.

V-Pin Wiring Verify that the V-pins are wired on the DR cards. For proper FrameScan Plus performance, connect at least one V-pin per driver/receiver card (32-node group) to the digital ground of the board under test.

See the **Fixturing Guidebook** for wiring details.

Replace FrameScan Plus Selector Boards When the system 5 volt power supply exceeds the level of the 5 volts generated on the FrameScan Plus Selector Card, CapScan and FrameScan Plus measurements can become unstable. If your system is producing unstable CapScan or FrameScan measurements, replace the Rev 1.3 or below FrameScan Plus Selector boards with the latest revision.

Note: This applies to systems with a DeltaScan II (PN 090-327-00) or DeltaScan II with Disconnect (PN 047-081-xx)—Z1890, Z1888, Z1884, Z1880, Z1866, Z1860, and Z1803—and fixtures with a FrameScan Plus Selector Card Rev 1.2 or higher.

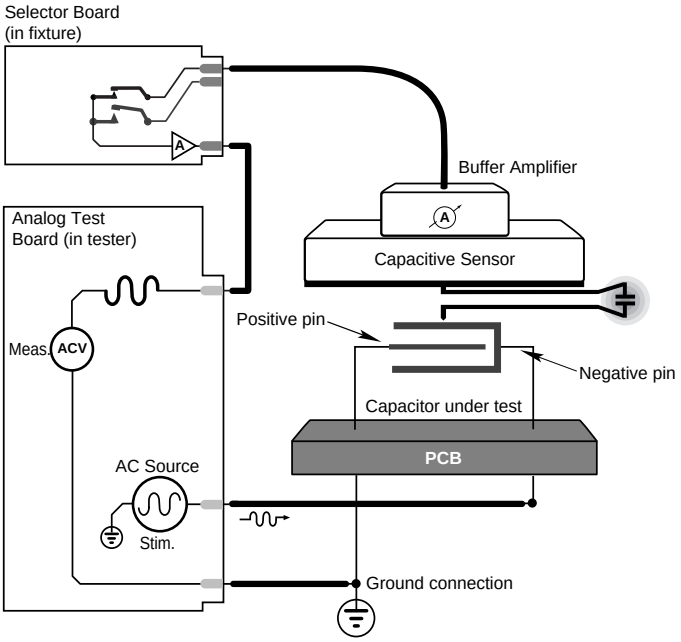
❖❖

CHAPTER 5 CAPSCAN

CapScan is a technique that tests for correct orientation of polarized capacitors on circuit boards. A stimulus signal is sent to each end of the capacitor in turn. A sensor mounted above the capacitor detects the signal in each case. Comparing the signal levels indicates whether the capacitor is oriented correctly or not.

Theory of Operation

In testing capacitors, CapScan sends separate stimulus signals to the expected negative and positive connections of the capacitor. With each stimulus, a sensor capacitively couples the radiated signal into the sensor, which returns a measurement. If the ratio of the expected negative pin signal to the expected positive pin signal is greater than a specified threshold value, the capacitor is correctly oriented; otherwise, it is not.



Measurement Formulas

The ratio for correct orientation can be expressed by the following formula:

Vneg. pin / Vpos. pin > Threshold Value (default 1.1)

Conversely, the ratio for incorrect orientation can be expressed by the following formula:

Vneg. pin / Vpos. pin < Threshold Value (default 1.1)

The default threshold ratio is 1.1 to 1, as discussed later in this chapter.

Test Constraints

Flexible Capacitors CapScan is more effective with SMT and axial electrolytic capacitors, which have predictable locations, than with flexible capacitors such as bead (teardrop) tantalums and radial electrolytics that have a range of possible positions because of their tendency to be bent over.

Capacitors with Low Impedances Because large-value capacitors present low impedances, even at low stimulus frequencies, the ratio of the two measurements may be too small to be meaningful with large-value capacitors over 1,000 µF.

Capacitors in Parallel If a large-value capacitor is in parallel with a small-value capacitor under test, the large-value cap will interfere with CapScan tests on the small-value cap.

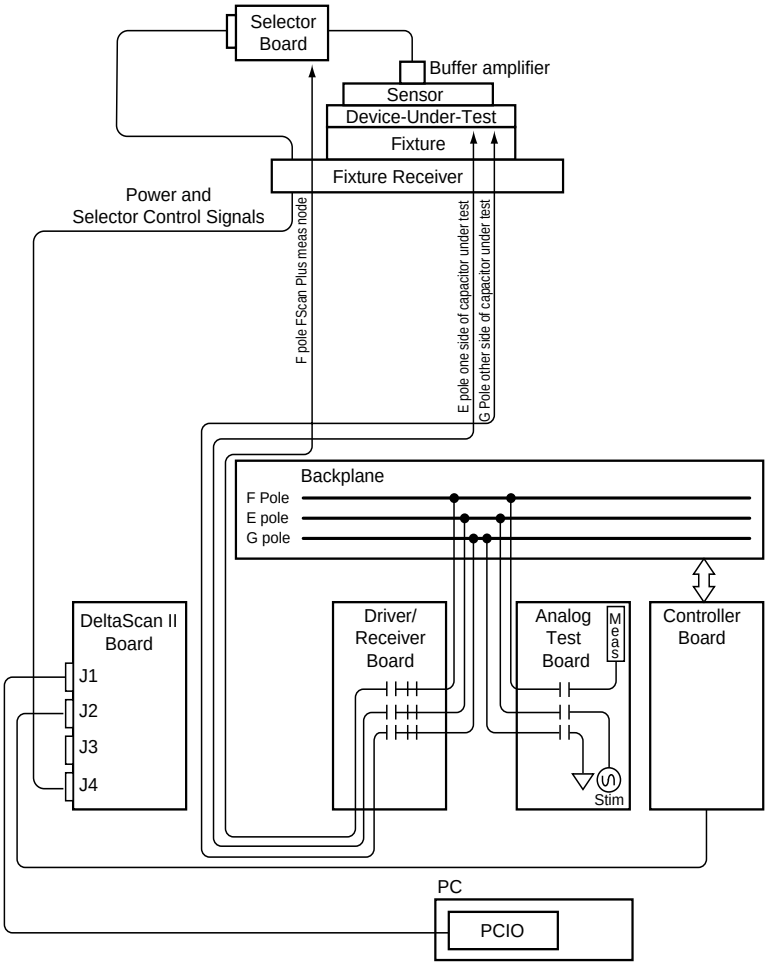
CapScan Hardware

CapScan uses the Analog Test Board (ATB), the standard Z18xx instrument for stimulus and measurement. Additional hardware requirements for CapScan consist of:

- Fixture-mounted selector board for selecting the sensors
- CapScan sensor/buffer assembly over each device to be tested
- DeltaScan II board and cable for controlling the selector board

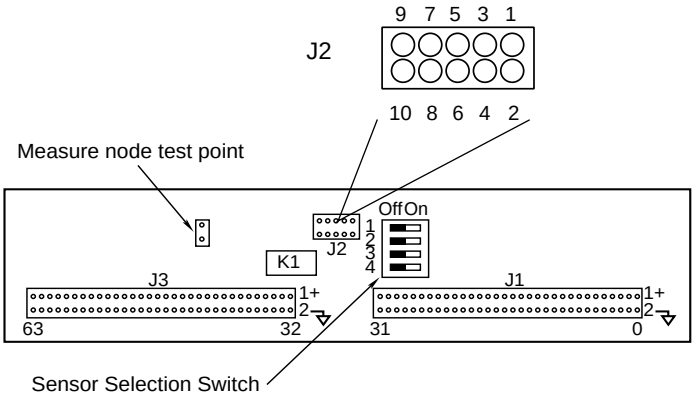
Note: Make sure that the tester contains a DeltaScan II board, not the older DeltaScan I version.

The following diagram shows the connections between the ATB, the sensor/buffer assembly, and the DeltaScan II board. Information on specific fixture wiring can be found in the **Z1800-Series Fixturing Guidebook**.



Selector Board

The selector board (PN 051-065-00) is the part of the CapScan-equipped fixture that switches the AC signal from sensor to sensor as required by the CapScan test.



Inside the tester, a cable routes the power and control signals from the DeltaScan II board to the fixture receiver. The signals pass via transfer pins through individual wires to a ten-pin jack, and through a ten-pin ribbon cable to J2 on the selector board.

Sensor Selection Switch States

Each selector board can accommodate up to 64 sensors and can be chained to additional selector boards up to a maximum of 1024 sensors.

Sensor groups are selected or deselected by address according to the position of the Sensor Selection Switch DIP, as shown at the right.

Sensor Group	Switch State: 4	3	2	1
0-63	Off	Off	Off	Off
64-127	Off	Off	Off	On
128-191	Off	Off	On	Off
192-255	Off	Off	On	On
256-319	Off	On	Off	Off
320-383	Off	On	Off	On
384-447	Off	On	On	Off
448-511	Off	On	On	On
512-575	On	Off	Off	Off
576-639	On	Off	Off	On
640-703	On	Off	On	Off
704-767	On	Off	On	On
768-831	On	On	Off	Off
832-895	On	On	Off	On
896-959	On	On	On	Off
960-1023	On	On	On	On

Selector Board Power and Control Wiring

The wiring path should be as follows: Z18xx fixture receiver pins to fixture pan TA row to transfer pins to ribbon cable to J2 pins on the Selector board.

The following illustration shows the fixture TA row pins to be wired to the selector board J2 pins. This information is also available in the **Z1800-Series Fixturing Guidebook**.

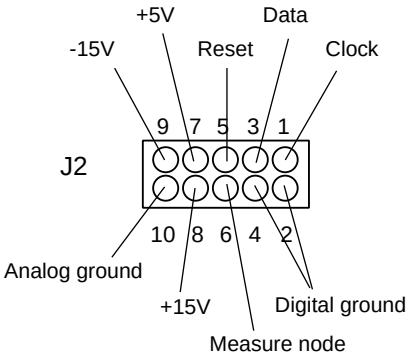
The selector board wiring from the fixture interface (row TA) to the fixture transfer pins must be correct. Individually check each fixture pin listed below with an ohmmeter.

WARNING! Be sure to remove the fixture from the tester interface before the wiring check because +15, - 15, +5, GND may be present at the interface.

Fixture TA Row Pins

```
     |0  22|
     |     |
     |     |
     |   25|
     |     |
     |5    |
+15V |6  28|DATA
     |7  29|RESET
-15V |8  30|CLOCK
     |     |
     |10   |
     |     |
     |     |
     |   35|
     |     |
     |15   |
 +5V |16 39|GND [Analog and
     |     |       Digital]
     |   40|
     |     |
     |21 42|
```

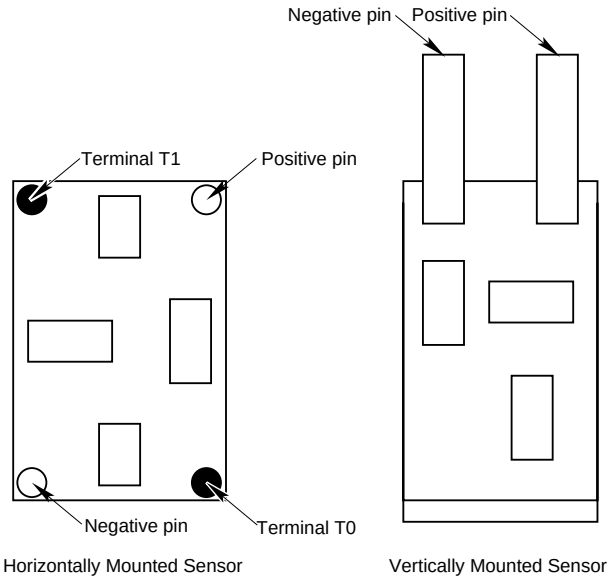
J2 Pins on Selector Board



Sensors

CapScan sensors can be mounted horizontal or vertical. The sensors are mounted in the fixture above devices targeted for test on the board under test. The sensors may be attached to an overclamp or they may be in the probe plate beneath the DUT (device under test).

- The horizontal sensor plate is composed of two physically separate plates: a metal ground plate and a metal signal plate. The signal plate is closest to the DUT.
- The vertical sensor plate is a single metal plate.



CapScan PRGMVARS

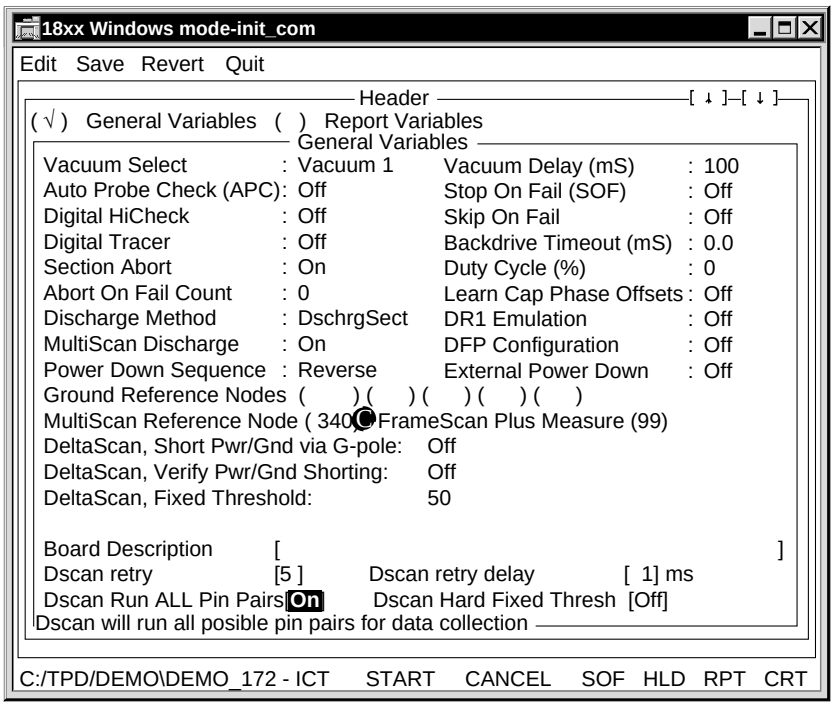
Header/PRGMVARS includes the following General and Report variables important to CapScan testing. If you use CapScan, check these variables.

For a description of all fields in Header/PRGMVARS, refer to the **Z1800-Series Programmer's Guidebook**.

General Variable

- **FrameScan Plus Measure**

  The FrameScan Plus Measure node is an otherwise unused node that lets you specify the measure node for FrameScan Plus and CapScan tests. The node is stored in the Header/PRGMVARS worksheet of the test program for the board. The default is 9999. This is the node that is hardwired to the output of the FrameScan Plus selector board. During a test, the FrameScan Plus Measure node is switched to the F pole.



CapScan variable

Report Variables

- **Report Meas Nodes**

  Off: The pin number is included in the report, but the node number is not included.

  On: The node number is included after the pin number in the report. The report includes one line per failing pin.

- **Report Values**

  Off: The report does not include any of the measured values.

  Actual: The report includes the actual measured values.

  Percent: If you select percent, the report includes actual values, since CapScan tests do not report percent.

  If Report Values is Actual or Percent the report includes one line per failing pin.

- **Report Limits**

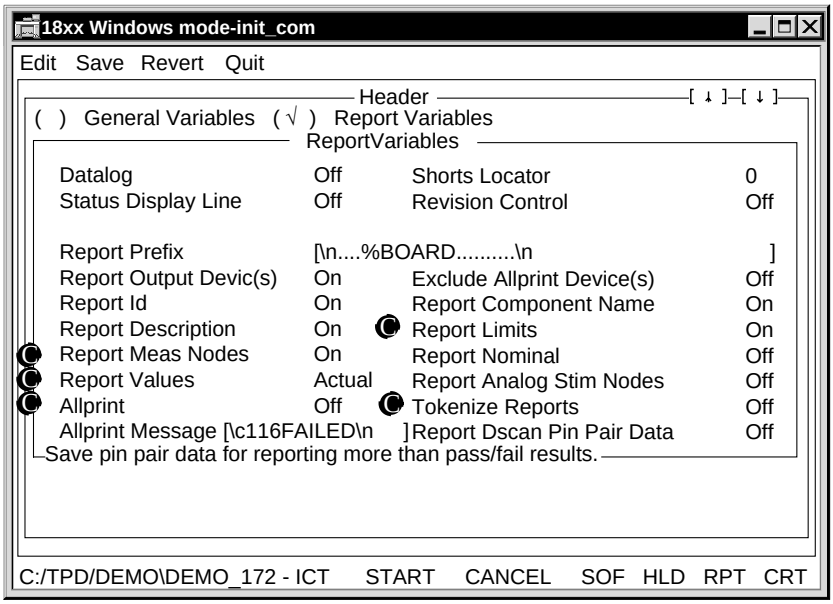
  On: The report includes the Pass/Fail limits of the test.

- **Allprint**

  On: A report is generated for every test, not just the failing tests.

- **Tokenize Reports**

  On: The Datalog and CRT reports are in Tokenlog format. The report file is TOKENLOG.DAT and is in the TPD\PROGRAM directory.



CapScan variables

Developing CapScan Tests

This section explains how to add CapScan tests to a new board test program.

- **To develop CapScan tests:**

  1. Set up CSCAN tokens.
  2. Update the PGEN.CFG file.
  3. Generate tests.
  4. Validate and troubleshoot tests.

Adding to an existing board test program To add a CapScan test to an existing board test program, follow the procedures outlined in the **Z1800-Series Programmer's Guidebook** for incremental test generation.

Note: If board topology has changed, run PGEN/Learn to reestablish the continuities, special cases, shorts, and merged special cases on the board.

Set Up CSCAN Tokens

The input list (IPL) is an ASCII file that contains a complete description of the board component parts and interconnections. For each CapScan test, modify the IPL syntax by adding an IPL record to support the CapScan test type.

IPL Record

A record is a section of the input list file IPL.DAT dedicated to a single component test step. Like all other component tests, a CapScan test is governed by its input list record.

Record syntax for a CapScan test:

Token	ID	Description	Name	X Sensor	Node List
CSCAN,	C7_A,	“CapScan Test”,	10nF,	X1,	97&98,45&317

Sensor Number The sensor number specifies which sensor to use for the capacitor to be tested. You must type an x in front of the sensor number to distinguish the sensor number from the list of node numbers.

Node List First node in the list is the first pin on the device, second node is the second pin, and so on for each pin on the device up to 625 pins. Use the number 9999 for an unconnected pin.

Note: For a six-wire test, both leads of the capacitor must be double-noded to allow remote sensing. See the example above.

Refer to the **Z1800-Series Programmer’s Guidebook**, Chapter 7, “Program Generator Tools,” for more information about record syntax in general.

Major and Minor ID Follow the Major/Minor ID convention for all components tested with both CapScan and other tests methods.

- The major ID is the part of the ID that comes before a dash or hyphen (-) or an underscore (_).
- The minor ID is any part after the major ID, including the dash or underscore.

In C7_A, for example, C7 is the major ID and _A is the minor ID.

Add a unique minor device ID to each new component entry. For example, use _CS, so that C7 becomes C7_CS. The major device ID, C7, will not be in conflict with C7_CS.

Update PGEN.CFG

Settings in the PGEN.CFG file configure the program generate function. You can edit the PGEN.CFG file to specify other CapScan test default values for PGEN to use instead of the standard defaults. For a complete discussion on editing the PGEN.CFG file, refer to the **Z1800-Series Programmer’s Guidebook**, Chapter 7, “Program Generator Tools.”

The following fields in the PGEN.CFG file apply to CapScan.

- **FSPMEAS**

  The Measure node is an otherwise unused node that lets you specify the measure node for a CapScan test. The node is stored in the Header/PRGMVARS worksheet of the test program for the board; the default designation is 9999.

Note: The FSPMEAS node is also used in FrameScan Plus tests. See Chapter 4 for more information.

- **CSCNRATIO**

  CapScan Ratio specifies the ratio of the strong to the weak signal in a CapScan test. The default is 1.1 to 1.

Build the Database File

Once edits are completed, save the IPL, and continue with these steps:

- **To build a new board test:**

  1. Run **PGEN/CLEAN**.
  2. Run **PGEN/BUILD**.

     This command creates a new temporary IPL database, IPL.DBF.

- **To build an existing board test:**

  Do NOT run PGEN/CLEAN. Run **PGEN/BUILD.**

  If you accidentally select PGEN/CLEAN, copy the board directory from your backup and start over.

Generate Tests

The PGEN/GENERATE command automatically generates the test program ICT.TST from the IPL. The process for developing and executing a test program that uses CapScan is the same as the existing processes for developing a Z1800-Series test program.

The three test generation methods are automatic program generation, incremental program generation, and manual program generation. They are described in the **Z1800-Series Board Test Tutorial**.

Important: The Programmer Efficiency Package (PEP) does not recognize CapScan tokens and will not perform an analysis on them in the input list.

- **To automatically generate a test:**

  1. Run **PGEN/GENERATE.**

     This command adds the IPL.DBF entries to the main test program ICT.TST.

     Important: Unlike other MultiScan techniques, which are added as “PwrOff” tests, CapScan tests are added as “Passive/Capacitor” steps.

  2. Run **PGEN/UPDATE.**

     This command is needed to finalize topology for all reports and before any Validates. The update is critical for success.

  3. After generating CapScan tests, review the resulting worksheets.

     Make sure that the Multi-Scan reference node, thresholds, nodes, etc. have been set correctly:

Validating and Troubleshooting Tests

The Validate process puts test steps through an automatic analysis process. Use PGEN/VALIDATE, your own analysis of system worksheets and reports, and a check of the CapScan hardware to achieve the best frequency and ratio for board conditions and eliminate false passes, false fails, and unstable tests.

Follow this process:

- Validate the tests.
- Look at the CapScan worksheets, Datalog and Tokenlog reports.
- Check CapScan hardware.
- Continue to run Validate and edit component and test attributes until you have the program perfected.

This section covers validating and troubleshooting suggestions, tools and processes. For complete information, also read Chapter 7, “Program Generator Tools” and Chapter 9, “Test and Debug Tools” in the **Z1800-Series Programmer’s Guidebook**.

Validate Tests

The Validate function attempts to improve CapScan tests by learning test parameters from a known good board. Validate finds the best operating frequency for the CapScan test and determines the ratio threshold to use for the Pass/Fail criteria.

Frequency CapScan tries to use AC2 (1.59Khz) as the stim frequency. If the value of the capacitor is too large (over 100uf) the stim current becomes too high at AC2 so Validate switches the operating frequency to AC1 (159 Hz).

Ratio Threshold Validate then does a CapScan test to determine what the F/R ratio is for the known good capacitor under test. A threshold is chosen which is half way between the measured ratio and a ratio of 1:1. For example, if the measured ratio was 1.8, then the threshold would be set to 1.4.

- **To validate the test program:**

1. Select **Validate** from the Setup menu.

   The system displays the Validate Configuration window.

2. Select **Validate CapScan**.

3. Using a known good board on the fixture, run **Validate**.

   Validate processes a CapScan test step in the same way whether you invoke Validate for the entire program, for the current section, or for the individual test step.

   To test a polarized capacitor for proper orientation, CapScan connects the E drive and E sense poles to the nodes associated with the positive lead of the capacitor. The G drive and G sense poles are connected to the nodes associated with the negative side of the capacitor, grounding this side of the capacitor. The F pole is connected to the output of the sensor amplifier via the selector board. An A.C. signal is applied to the capacitor via the E pole connection, and the amount of radiated signal is measured by the ATB via the F pole connection. This signal level is stored for later comparison.

   Next, the connections to the capacitor are reversed such that the signal is applied to the nodes associated with the negative lead, and the nodes associated with the positive lead are grounded via the G pole. A second measurement of the radiated signal is taken, and the ratio of the second measurement divided by the first is calculated. This ratio is compared to the F/R ratio threshold specified on the worksheet to determine if the test passes or fails.

Validate generates a report listing each parameter it changed. The report goes to the exception list file, EXCEPT.LST.

4 Troubleshoot any failures.

CapScan worksheets and reports provide information for troubleshooting tests. In addition, check the sensor board, the buffer/sensor, and fixture wiring for problems. See the following sections.

5 Revalidate individual devices as necessary to get repeatable and stable tests on the sample boards.

MultiScan Failure Flag A system flag called MultiScan Failure is set if any MultiScan test, including CapScan, fails. If the Section Abort feature is enabled, a failure causes the software to jump to the Trailer.

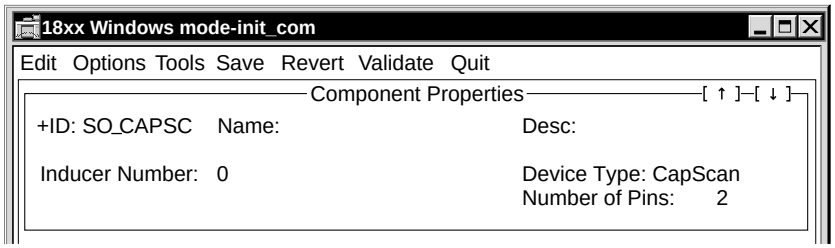
Troubleshoot Tests

This section contains suggestions for making test program corrections. Start troubleshooting by examining the test worksheets and reports.

Edit CapScan Worksheets

Use the properties and controls of the CapScan worksheets to troubleshoot tests.

Component Properties Section The Component Properties section of a CapScan worksheet specifies the information required to generate a CapScan test for a component. You previously set up the information by running Build and Generate on the IPL or manually adding a CapScan component and filling in the information on the worksheet.



Component Properties Fields

- **ID**

  Component identifier. For example, “C7_Cs.” The + preceding the ID indicates that the step is enabled.
- **Name**

  Device name.
- **Desc**

  Text description of the test. For example, “CapScan test for C7.”
- **Device Type**

  CapScan. If the test fails, check this value.
- **Number of Pins**

  Total number of pins on the component. The default value is two (2).
- **Node Entry**

  The Node Entry box pops up when you click on the number in the Number of Pins field. Two nodes are required for each pin.

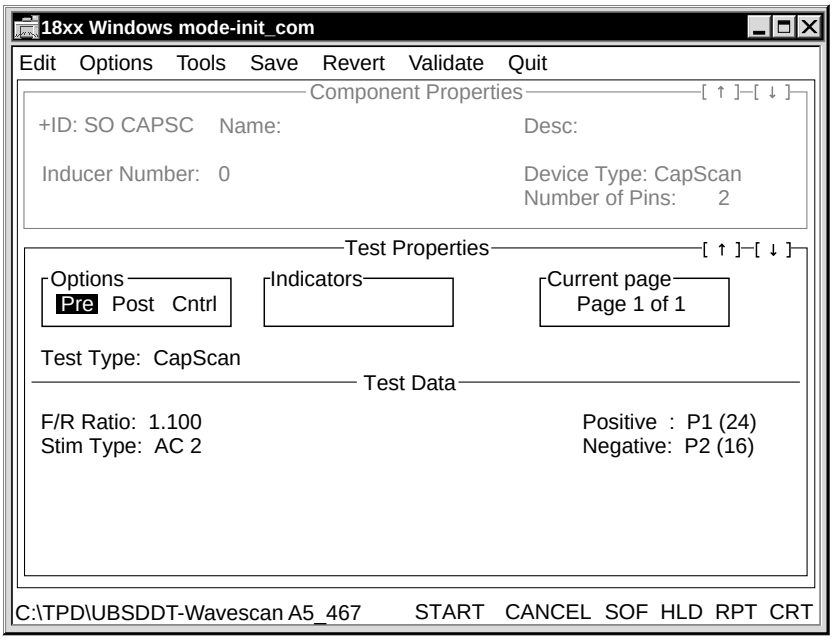
  Is each pin node in the worksheet correct?

- **Sensor Number**

  Enter an integer from 0 (zero) to 1023 to indicate which sensor to use to measure the capacitor being tested.

  If the test fails, make sure that the correct sensor number is recorded in the worksheet. Locate the sensor over the part; follow the positive pin and negative probe pin wiring to the selector board; observe the position of the wires on the selector board connector J1 or J3. Sensor numbering starts at with zero. Sensor number 0 is the first physical position on connector J1 of board 1.

Test Properties Section The Test Properties section of a CapScan worksheet displays test parameters and results. From here you edit and execute the test step.



Test Properties Fields

- **Options**

  Displays the Pre-Test, Post-Test, and Test Page Control options.
- **Test Type**

  CapScan.
- **Indicators**

  There are no indicators for a CapScan test.
- **Current Page**

  CapScan tests have one page only.

Test Data Fields This section displays test results that can be edited.

- **F/R Ratio**

  Expected threshold ratio between the two stimulus results; the default value is 1.1 to 1.

Note: A threshold value that is set too low may lead to false passes during tests.

- **Stim Type**

  Type of stimulus to be applied, AC 1 or AC 2. The default value is AC2 when the worksheet is generated; however, Validate selects the best stimulus frequency for the device under test (DUT).

- **Positive, Negative**

  Specify which pin is connected to the positive lead of the capacitor and which to the negative.

Review CapScan Output

CapScan output includes CapScan Datalog/CRT report and CapScan Tokenlog report.

CapScan Datalog/CRT Report When you execute a CapScan test from Run mode, the software generates a report. If Allprint is On, the report includes both passing and failing tests. If Allprint is Off, the report is limited to the failing tests.

CapScan Tokenlog Report CapScan test results are logged by Tokenlog if you select Tokenlog in the Setup-Data-Program Execute channels pop-up window. If you select Tokenize Reports from PRGMVARS, the Datalog/CRT report will be in Tokenlog format. The report file is TOKENLOG.DAT and is in the TPD\PROGRAM directory.

E-nodes are reported twice.

Check Hardware

This section is a guide to troubleshooting the sensor board, buffer/sensor, and fixture.

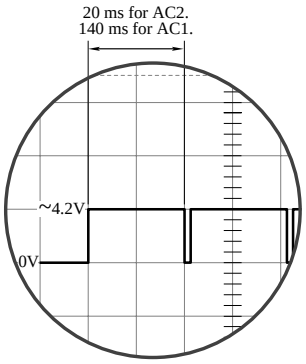
Selector Board Settings

- **Sensor Selection Switch Settings**

  Make sure that the binary switch on the selector card is set correctly. The switch settings should match the table on page 5-3.

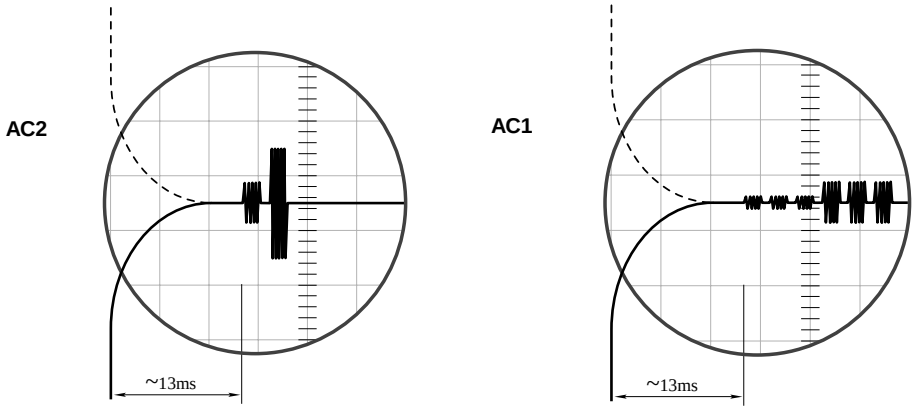
- **Correct Sensor**

  Make sure that the correct sensor is selected by the card. Put the worksheet in Repeat mode. Connect an oscilloscope probe on the positive pin of the buffer board. A 4.2-volt signal should appear on the scope display when the sensor is correctly selected, as illustrated below.



- **Correct Signal**

  Make sure that the signal from the selector board is as expected. Put the worksheet in Repeat mode. Connect an oscilloscope probe on the selector board test point. The signal on the scope display should appear as illustrated below.



Buffer/Sensor Check the sensor to make sure that a strong signal is produced at the buffer output when the sensor is close to a signal source. To do this, use a FrameScan test. FrameScan gives results in terms of the signal strength measured. (CapScan provides the ratio of two signals rather than signal strength measured.) To set up a FrameScan test, refer to “Check the Buffer/Sensor” on page 4-16.

Fixture Wiring

- **Ribbon Cable**

  Check that the cable from the transfer pins to J2 on the selector board is oriented correctly and securely plugged in.

- **Buffer Circuit Positive/Negative Probe Wiring**

  Selector connectors J1 and J3 are on the top side of the selector board. Pins closest to the edge of the board are even numbered pins. Pins away from the edge of the board are odd numbered pins. See the CapScan Selector Board drawing on page 4-3.

  Observe the orientation of the buffer circuit and identify the positive pin and the negative pin. The positive pin should be wired to an odd numbered pin of connector J1 or J3, and the negative pin wired to an even numbered pin of connector J1 or J3.

- **Measure Node Wiring**

  The FSPMEAS measure node should be wired **only** from an unused node, through transfer pins, to selector board connector J2’s pin 6. There should be no other wires connected to the measure node.

- **Selector Board Power and Control Wiring**

  The wiring path should be as follows: 18xx fixture receiver pins to fixture pan TA row to transfer pins to ribbon cable to J2 pin on selector board.

  The selector board wiring from the fixture interface (row TA) to the fixture transfer pins should be correct. Individually check each fixture pin with an ohmmeter. See “Selector Board Power and Control Wiring” on page 5-3 for the pin numbers and locations.

Replace FrameScan Plus Selector Boards When the system 5 volt power supply exceeds the level of the 5 volts generated on the FrameScan Plus Selector Card, CapScan and FrameScan Plus measurements can become unstable. If your system is producing unstable CapScan or FrameScan measurements, replace the Rev 1.3 or below FrameScan Plus Selector boards with the latest revision.

Note: This applies to systems with a DeltaScan II (PN 090-327-00) or DeltaScan II with Disconnect (PN 047-081-xx)—Z1890, Z1888, Z1884, Z1880, Z1866, Z1860, and Z1803—and fixtures with a FrameScan Plus Selector Card Rev 1.2 or higher.

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