TERADYNE Z1800-Series

Board Test Tutorial

Teradyne, Inc.
Assembly Test/Walnut Creek
2625 Shadelands Drive, Walnut Creek, CA 94598-2597
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Teradyne, Inc.
Assembly Test/Walnut Creek
2625 Shadelands Drive
Walnut Creek, CA 94598
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BOARD TEST TUTORIAL

Manual History

- First Edition, October 1998, Version F.2b

Publications No. 1800M246

2625 Shadelands Drive · Walnut Creek, CA 94598 · (925) 932-6900
Customer Service Hotline (800) 457-8326

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BOARD TEST TUTORIAL

You can use various approaches to build an in-circuit test program, based on the materials available to start the process. For instance, board tests that are developed using CAD generated data are developed differently from board tests that have no CAD data.

- With CAD data you can develop the fixture and program in parallel until the validation phase, when you need the fixture to run Validate, an interactive verification tool.
- Without CAD data you enter components by hand.

It is best to build the fixture first so you can use it to generate the program one component at a time.

Refer to the **Z1800-Series Fixturing Guidebook** for detailed information about fixtures.

Refer to the **Z1800-Series Programmer's Guidebook**, Chapter 5, for more information.

Overview

You can use this tutorial to learn how to:

- Develop test programs for your Z1800-series tester.
- Navigate the Z1800-series Step Worksheets.

Tutorial Conventions

Every effort has been made to be consistent with the terminology and special text elements used throughout this tutorial. As a rule the following conventions are used to make your learning easier.

Instructions

When you begin the tutorial, the steps you follow are fully explained, such as: Move your mouse pointer to the ID field and type R14. As you progress through the tutorial, the instructions become more direct, such as: Type R14 in the ID field.

Menus

Menu selections are presented either in menu bar or pull-down formats.

The example below shows both formats: the horizontal Main menu bar and the vertical pull-down Files Menu. When you are asked to make a selection from a menu that has opened as a result of a selection from another menu, the selections are separated by slashes.

In the example: **Edit/Intc/Jumpers**

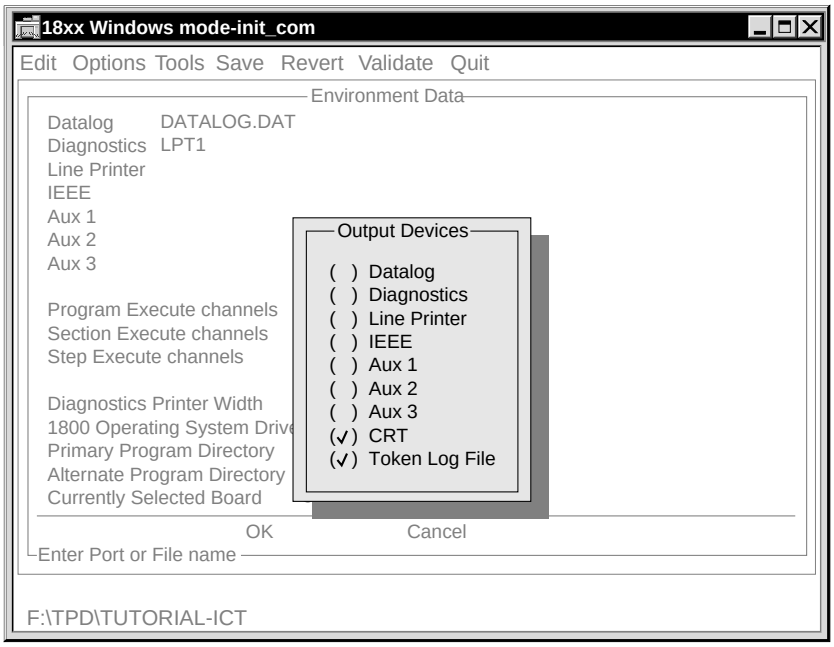
Edit is the Main menu bar selection.

Intc is in the menu bar that opens when you click Edit.

Jumpers is in the pull-down menu that opens when you click Intc.

Pop-up Windows

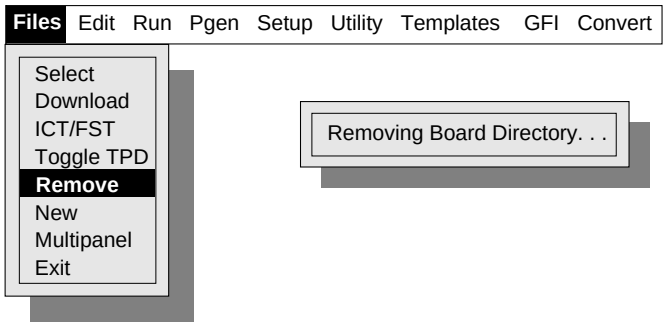
Pop-up windows are used to show menus, output, queries, system dialog and process messages, and lists. A pop-up window overlays the active view as shown in the following example.



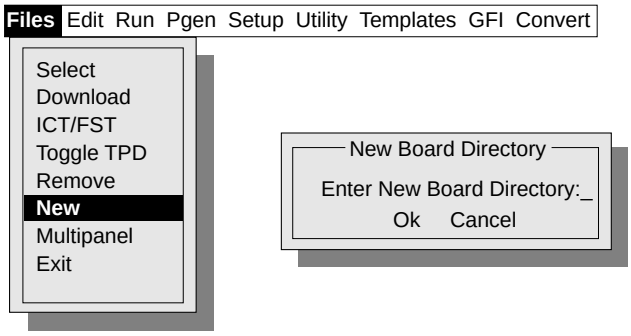
- You can drag a pop-up window to another location.
- You can resize of a pop-up window by clicking one of its corners and dragging it.

Process Windows and Dialog Boxes

The software system delivers process and dialog messages through a set of windows. Most process windows are visible for the short period of time required to communicate the information. In the example below, Removing Board Directory, is a process message that is shown briefly when you remove a board directory.



A dialog box requires some kind of input from you. In the example shown below, after selecting **New**, you are prompted to either type a response and click **OK**, or click **Cancel** to exit the box.



Menu Selections

You can select from a menu using:

- The mouse,
- The keyboard, or
- A combination of both.

Users familiar with mouse operations will have no trouble with clicking and pull-down operations.

- Click one of the Main menu bar categories and the pull-down menu of commands opens.
- Click a command from the pull-down menu to select it, or type the red letter in the command (red is the default color).
- Navigate through the pull-down menus using the keyboard up or down arrow keys, then press Enter to open the selected menu or menu item.

Step Worksheet Selections

You can use both the mouse or keyboard to perform edits in the Step Worksheet. Click an item to initiate an action or use the keyboard shortcut.

Component Select Window Selections

You can open a Step Worksheet from the Component Select window using either the mouse or the keyboard:

- Click the appropriate component with the mouse, or
- Use the keyboard arrow keys to select the appropriate component, then press Enter.

Moving and Selecting in Component Properties

After you have selected a component from the Component Select window, the component's Step Worksheet opens to the Component Properties portion or the Step Worksheet. Use the mouse to navigate through the Step Worksheet.

Click an item or field to:

- Select it and type new text.
- Open a pop-up list where you can use the mouse to select an item such as Device Type, Value, Scale, and so on/
- Open a pop-up window where you can enter information such as Number of Pins.

To close a window, click anywhere outside the window. You must close a window before selecting Save; otherwise your changes are not be saved.

Moving and Selecting in Test Properties

The Test Properties portion of the Step Worksheet is opened after you click **Generate Test** from the Tools menu. Test Properties navigation techniques are the same as those used for Component Properties.

Program Generation Overview

Before you begin the tutorial you should have the following:

- Version F.2b system software installed on your PC.

  Refer to the **Z1800- Series Computer Configuration And Software Installation Guide** for complete instructions.
- The self-test fixture provided with the tester. In this tutorial you will use the self-test fixture as both the bare board and the loaded board.
- The schematic for the self-test fixture (PN 045-253-00 or PN 051-047-00). Refer to your tester's engineering reference drawings manual.

To start the tester and verify that it is working properly:

1. Turn on the AC power and wait 30 minutes for warm-up.
2. Install the self-test fixture.

   To run diagnostic tests, you must use the Z1800-series system software.
3. Type **18start** at the command prompt to start the system software.
4. Select **Utility/Diagnostics** to open the Diagnostics interface.
5. Click **Individual** or **Chain** as the diagnostic test mode (Run mode).

Refer to the **Z1800-Series Maintenance Reference**, Chapter 2, for information about running diagnostics.

Creating a New Board Program Directory

Z1800-Series system software consists of three main directories:

- TPD
- MOS
- PGT

The TPD directory contains test programs. If you load the Z1800-Series system software on your C drive, the new board program directory you create in this tutorial resides in C:\TPD.

Tutorial References

The following references are in the **Z1800-Series Programmer's Guidebook**, Chapter 1.

- Files and Directories for an overview of the Z1800-Series system software's file and directory structure.
- Managing Test Programs for a list of Files menu selections.
- Managing Test Programs, Creating a New Program for a discussion of the selection New in the Files menu.
- Setting Log on and Permissions.

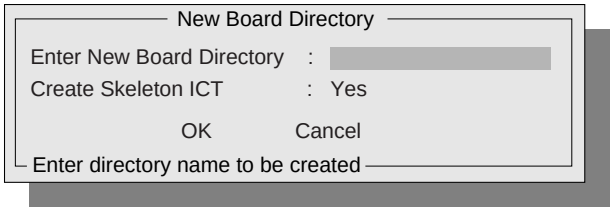
Exercise: New Board Directory

Create a new board program directory to begin the development of a test program:

1. Log on to the Z1800-series system software as Supervisor.

   If Supervisor is not the default log on, click **Supervisor** and enter the correct password.
2. From the Main menu bar, click **Files**.
3. From the Files pull-down menu, click **New**.

   The New Board Director dialog box opens.



4. In the Enter New Board Directory field, type **tutorial**.
5. Click **OK**.

   You now have a empty program that you can open with the editor.

The following sections of this Tutorial explain how to fill the empty program with component and test data.

Learning Interconnect Information

You use the PGEN (program generator) menus to create test programs automatically (autogeneration) from menu selections using input list and template library data.

Refer to **Z1800-Series Programmer's Guidebook**, Chapter 7, for information about the PGEN submenu.

Automatic Program Generation

Using an input list to generate a program automatically is the most common way to develop programs. The process begins with complete component information in the form of an input list. The input list either is derived from CAD data files or is created by hand using an editor.

Refer to **Z1800-Series Programmer's Guidebook**, Chapter 6, for more information.

Adding Individual Tests

A test program for a board-under-test consists of

- Control functions

  The Header and Trailer sections of the program contain the control functions.
- Component tests.

  The individual test steps contain the component test data.

This part of the tutorial explains how to use the Edit menu bar functions to enter data for the component tests. Component data is entered into the board test in the following sequence:

- Interconnects (Jumpers, Continuities, Shorts)
- Passive (Inductors, Capacitors, Resistors)
- Semi (Diodes, Transistors, Zener Diodes)
- PwrOff (Analog Power-Off devices and MultiScan)

- Board Power (Power_On and Power Bus measurements)
- Linear (Analog Power-On devices)
- Digital (Gray code and Vector)

The procedure for entering component information is similar from one device to another. Where the procedure is virtually the same within a category of components, such as inductors, capacitors, and resistors, the instructions focus on only one of those components.

Interconnects

The Interconnect menu contains the following component sections in the order they are run during production testing:

- Discharge
- Jumpers
- Continuities
- Ignores
- Merges
- Shorts
- Opens

Jumpers

The tester learns continuities from a bare board and ignores from a loaded board. If your board has any jumpers, they are included with ignores and are not tested.

Components such as very low value resistors or inductors are also entered as jumpers. If they are not entered as jumpers, these components can give false shorts failures during the shorts test algorithm.

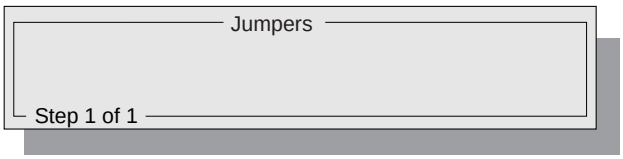
Refer to the **Z1800-Series Component Test Reference** for more information about jumpers tests.

Exercise. Entering a 1 ohm resistor as a jumper.

In this part of the tutorial, enter R14, a 1 ohm resistor, as a jumper.

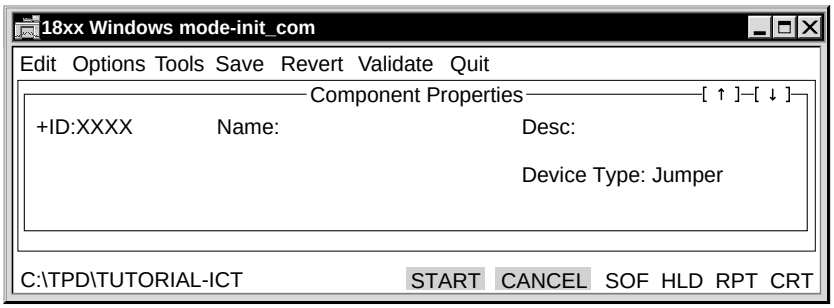
1. From the Main menu bar, click **Edit** to open the Edit menu bar.
2. Click **Intc.**
3. Click **Jumpers** and the Jumpers Component Select window opens.

   If this is the first time you have used Tutorial, the window is empty.



   If there are other components listed in the window, you must select the location where you want to add your new component. New components are added in sequence, left to right; therefore, click an existing component, press Enter, and the new component is added to the left of it.

4 Click **Add** from the menu bar to add a jumper, and the Component Properties portion of the Step Worksheet opens.



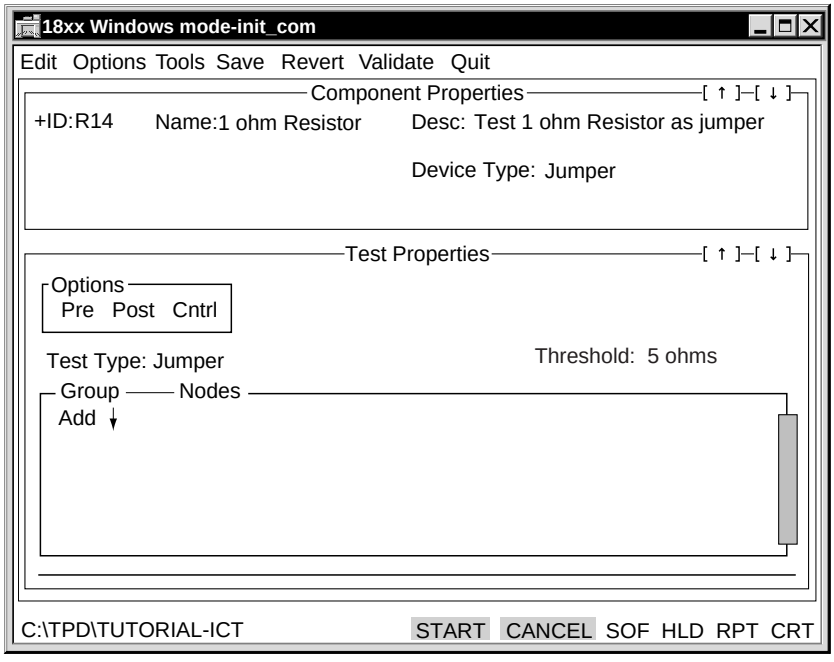
To edit the Component Properties portion of the Step Worksheet:

1 Move your mouse pointer to the ID field and type **R14**.
2 Press Enter to advance to the next field.
3 Type **1 ohm resistor** in the Name Field
4 Type **Test 1 ohm resistor as jumper** in the Desc field.
5 Click **Save** from the menu bar.

To edit the Test Properties portion of the Step Worksheet.

1 From the menu bar, click **Tools**.
2 Click **Generate Test**.

A jumper Test Properties page opens below the Component Properties portion of the Step Worksheet.



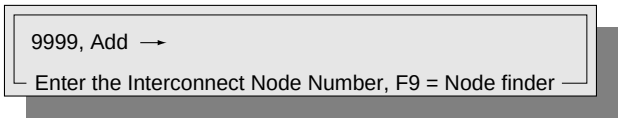
The Threshold field shows the default value of 5 ohms.

Since the default number of jumpers is 0, you must add the jumper to Test Properties.

1. Click **Add** in Test Properties.

   A row opens under Group/Nodes showing Group 1 with the dummy node 9999.

2. Click in the row to open the Interconnect Nodes Number entry box.

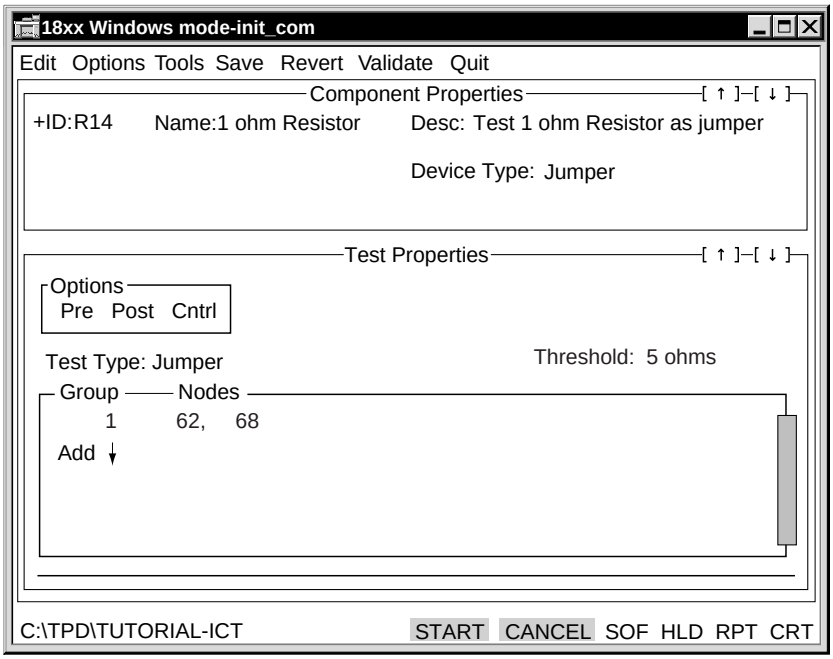


3. Move the pointer to 9999 and type **62** for the node number.
4. Press **Enter** twice.

   The first time you press Enter, ADD is selected; the second time a field is selected where you type another node number.

5. Type **68**, then press **Enter**.
6. Move the pointer outside of the entry box and click.

   The Interconnect Node Number entry box closes and the node numbers are entered for Group 1.

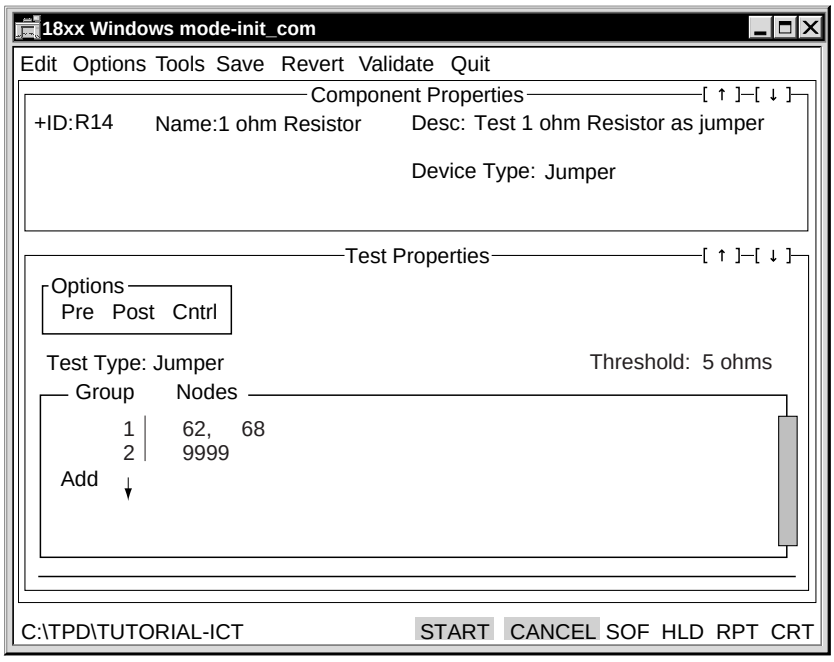


7. Click **Save** from the menu bar, to update the test step.

If a single jumper ID connects more than two nodes, you can add node numbers to the chain in Test Properties:

1 Press **Enter** twice.

Another row is added to Group/Nodes.



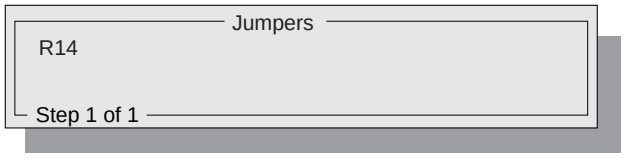
2 Type the node number, following the procedure you used for Group 1.

3 Press **Enter** for each additional node.

An additional node number field is highlighted each time you click Add or press Enter. You can make this chain as long as required. The resulting test FAILS if any of the points in a jumper chain are open. You can delete a point in a chain without reentering the whole chain by entering a space for its node number, then pressing F10.

4 Click **Quit** to exit the Step Worksheet.

Notice that the Jumper Component Select window now lists R14, the jumper you just added.



Passive: Inductors, Capacitors, Resistors

In this part of the tutorial, you will use Component Properties to enter component names, parameters, and connections. In the first exercise you will create a Step Worksheet for a resistor. In the second exercise, you will add a parallel RC network.

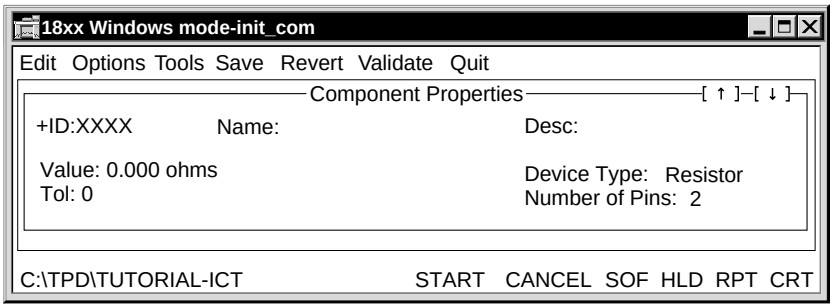
Refer to the **Z1800-Series Component Test Reference** for information on resistor testing.

Exercise. Create a Step Worksheet for a resistor.

Make sure you are at the Edit menu bar. If you are still at the Intc menu bar, click **Quit** until you return to the Edit menu bar.

1. Click **Passive**.
2. Click **Resistors**.

   The Resistors Component Select window is opened.
3. Click **Add** from the menu bar, and the Component Properties portion of the Step Worksheet opens.



You must enter data in **ID**, **Device Type**, **Value**, and **Tolerance**, and **Nodes** in Number of Pins field pop-up window. The Name and Description fields help identify the component, but they are not required for test generation.

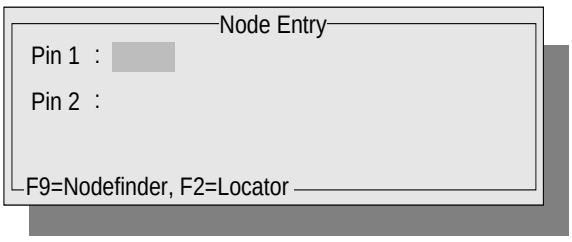
1. Type **R28** in the ID field.
2. Type **10 Kohm.1%** in the Name field.
3. Type **Sample resistor test** in the Description field.

To enter data for Value field:

1. Type **10** in the Value field.
2. Click the units portion of the Value field, and the Value pop-up list opens.
3. Click **Kohms**.

To enter node numbers for pins:

1. Click the **Number of Pins** field, and the Node Entry window opens.



2. Type **67** for Pin 1.
3. Type **84** for Pin 2.
4. Click outside the window to close it.

   You don’t have to decide which pin is Stim and which is Meas at this time. You can swap them during test verification using the Swap Poles command from the Tools menu.

5 Click **Save** to add the Test Step.

6 Select **Tools/Generate Test**, and the Test Properties portion of the Step Worksheet opens.

7 From the menu bar, click **Save** to save the test.

If you are at a tester, you can click Start to see the results of the measurement on the status line.

8 From the menu bar, click **Quit** to exit the Step Worksheet.

The resistor you just added, R28, is now in shown Component Select window.

If you are adding more than one new component, you do not have to Quit and click Add again from the menu bar. Click the up- down- arrows (↑ ↓) in the upper right of Component Properties, or your keyboards PG-UP/PG-DOWN keys, to add a new component Step Worksheet either before or after the current one. The Add function is only available after you have added a new component. This function is automatically disabled when you click Quit in the Step Worksheet.

Adding a Parallel RC Network

Now you can add a parallel RC network.

Refer to the **Z1800-Series Component Test Reference** for information on testing capacitors in parallel with resistors.

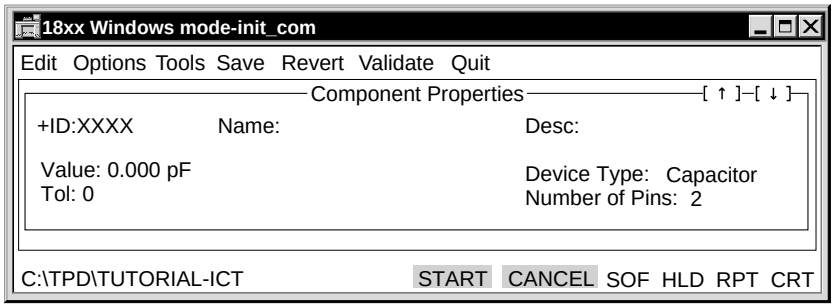
Exercise: Adding a test step for a parallel RC network

Before you begin this exercise, make sure you are at the Edit menu bar.

To edit Component Properties:

1 Select **Passive/Capacitors**, and the Capacitor Component Select window opens.

2 Click **Add**, and the Component Properties portion of the Step Worksheet opens.



3 Type **R19-C13** the ID field.

4 Type **10 Kohm & .01 uf** in the Name field.

5 Type **Parallel RC tes**t in the Description field.

6 Click the **Device Type** field to open a pop-up list.

7 Click **Resistor** for the Device Type.

The first page of an RC test must be the resistor test; this saves you future editing.

Enter a value for the resistor:

1 Type **10** in the Value field.

2 Click the units portion of the Value field, and a Value pop-up window opens.

3 Click **Kohms**.

4 Type **1** in the Tol field.

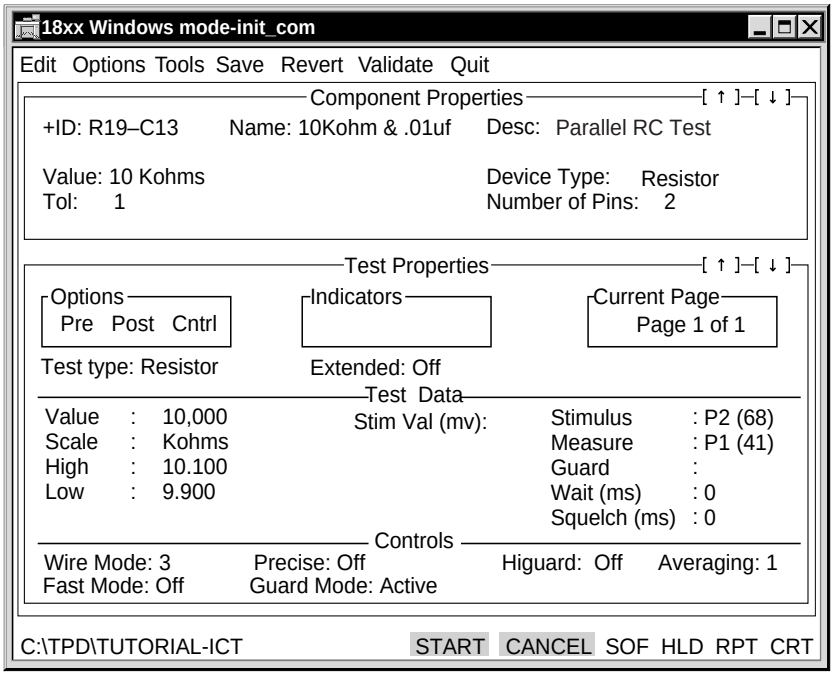
Enter pin numbers:

1. Click the **Number of Pins** field, and the Node Entry window opens.
2. Type **41** for Pin 1.
3. Type **68** for Pin 2.
4. Click outside the window to close it.
5. Click **Save** from the menu bar to add the Test Step.

To edit the Test Properties portion of the Step Worksheet:

1. Select **Tools/Generate Test**.

   The new Test Properties page opens below the Component Properties portion of the Step Worksheet.



2. Select **Tools/Add Page**.

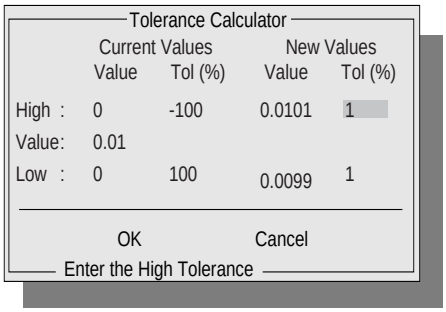
   The Current Page is 2 of 2.
3. Click the **Test Type** field.
4. Click **Capacitor** from the Test Type pop-up list.
5. In the Test Data section of Test Properties, type **0.01** in the Value field.

   When entering decimals, you must type a digit before the decimal.
6. Click **uf** from the Scale pop-up list.

Set the high and low limits in Test Properties:

1. Select **Tools/Tolerance Calculator** from the menu bar.

   The Tolerance Calculator sets the high and low limits in Test Properties automatically.

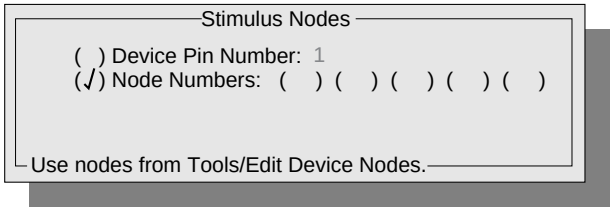


2. Under New Values, type **5** for the High Tol (%).
3. Under New Values, type **5** for the Low Tol (%).
4. Click **OK** and the Tolerance Calculator window closes.

   In the Test Data section of Test Properties, High is set at 10.500 and Low is 9.500. Scale is set to nf.
5. Click **On** for RC Mode field.

Set the Stimulus node:

1. Click to the right of **Stimulus** to open the Stimulus Nodes dialog box.



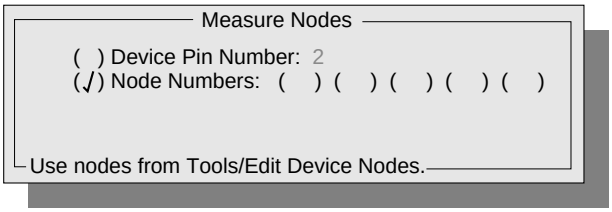
2. Click in the parentheses of **Device Pin Number**.

   Allow Pin 1 to remain as the default.
3. Click outside the box to close it.

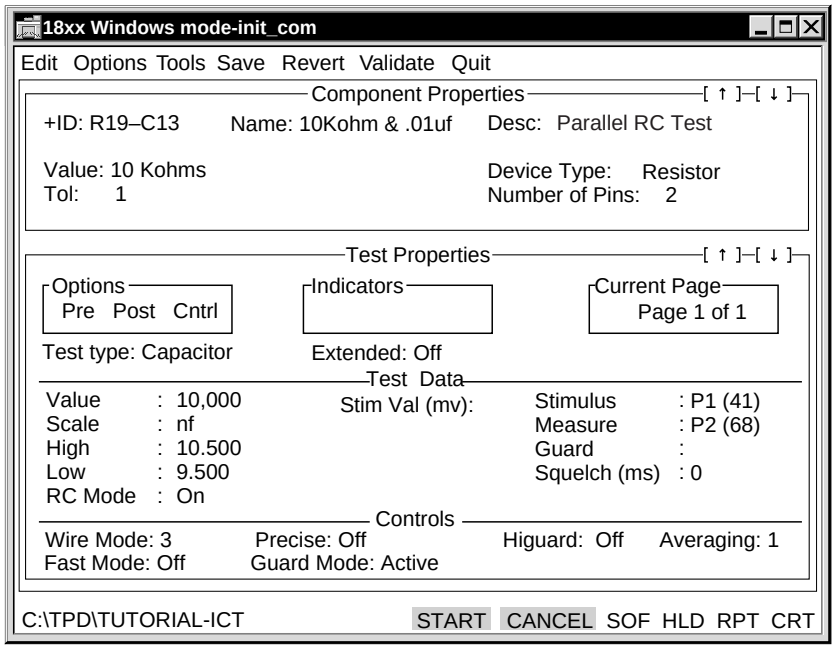
   P1 (41) appears in the Stimulus field.

Set the Measure node:

1. Click the **Measure** field and the Measure Nodes dialog box opens.



2. Click in the parentheses of **Device Pin Number**.
   Allow Pin 2 to remain as the default.
3. Click outside the box to close it.
   P2 (68) appears in the Measure field.



4. Click **Save** from the menu bar to update the Test Step.

To run the resistor test:

1. Click the up arrow located in the upper right of the Test Properties portion of the Step Worksheet.
   The Current Page is 1 of 2.
2. If you are at a tester, click **Start** to see if the resistor test passes.

To run the capacitor test:

1. Click the down arrow in Test Properties.
   The Current Page is 2 of 2.
2. If you are at a tester, click **Start** to run the capacitor test.
   To get a valid test result for the capacitor, check the result of the resistor test on page 1.

To update the component database:

1. Click **Quit**.

   If prompted, click **Yes** to add or update the step.

   The Capacitor Component Select window opens listing R19-C13.
2. Click **Quit** until you return to the Main menu bar.
3. Select **Pgen/Update** to update your component database.

Semi: Diodes, Transistors, Zener Diodes

In this section you will add a transistor to your test program, then add a page as a beta (gain) test.

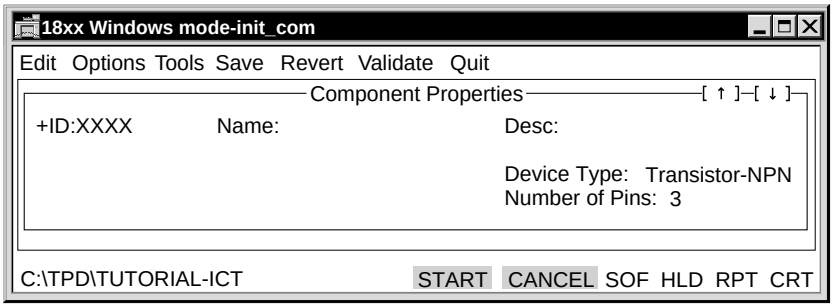
- To add diodes, transistors, and zeners to a test program, you must know the anode and cathode for diodes and zeners, or the emitter, collector, and base nodes of the component.
- To test transistors, the program tests the junctions (Transistor Test Type), and gain (Beta Test Type). This test finds incorrect or missing transistors as back-to-back diodes.
- Transistors require multipage tests, so that one page tests the base-emitter junction and another page tests the base-collector junction.
- The beta test page is added after you have created the junction test.
- On axial lead diodes, a band indicates the cathode. For transistors, you may need to refer to the data sheet or to the board's schematic to determine the leads.

Refer to the **Z1800-Series Component Test Reference** for information on transistor testing.

Exercise: Create a test step for a transistor.

Before you begin this exercise, make sure you are at the Main menu bar.

1. Click **Edit**.
2. Click **Semi**.
3. Click **Transistors**.
4. Click **Add** from the menu bar, and the Component Properties portion of the Step Worksheet opens.

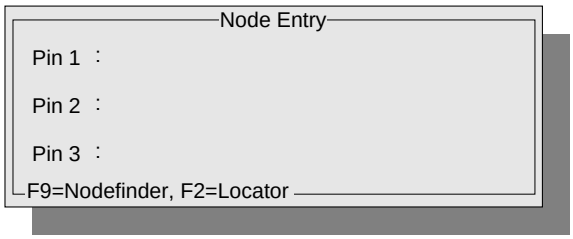


5. Type **Q1** in the ID field.
6. Type **2N2222A** in the Name field.
7. Type **Sample transistor test** in the Desc field.

Transistor-NPN is the default for the Device Type, and 3 is the default for the Number of Pins field. You do not have to change these selections.

You will enter nodes representing the three leads of the transistor base, emitter, and collector in that sequence. The collector must be a sense node for the beta test you will create in the next exercise.

1. Click to the right of **Number of Pins** and the Node Entry box opens.



2. Type **9** for Pin 1.
3. Type **1** for Pin 2.
4. Type **84** for Pin 3.
5. Click outside the Node Entry window to close it.
6. Click **Save** from the menu bar.
7. Select **Tools/Generate Test**.

   Note that in this instance, Test Properties has two pages because two tests were created—a forward voltage test and a reverse leakage test.

To see the test results for page 1:

1. Click **HLD** in the lower right corner.
2. Click **Start**.

   The status shows the results for the reverse leakage test.
3. Click **Start**.

   A message in the lower right corner indicates the forward voltage test for the base-emitter junction passes.
4. Click **Cancel**.

To see the test results for page 2:

1. Click the down arrow in the upper right corner of Test Properties to open page 2.
2. Click **Start**.

   The status shows the results for the reverse leakage test.
3. Click **Start**.

   A message in the lower right corner indicates the forward voltage test for the base-collector junction passes.
4. Click **Cancel**.
5. Click **HLD** to deselect it.

   A passing standard transistor, or junction, test confirms the presence of the transistor device on the board. The beta, or transistor gain, test verifies the device is correctly oriented.

Transistor Beta Test

In this part of the tutorial you will add a beta test to the transistor test you just created.

The transistor beta test measures the DC current gain to determine if the component is properly oriented and is operating. The beta test may not work in all circuit configurations due to the possible influence of surrounding components. Both junction and gain tests can be performed on the same component.

To create a beta test, add a page to the transistor Test Properties:

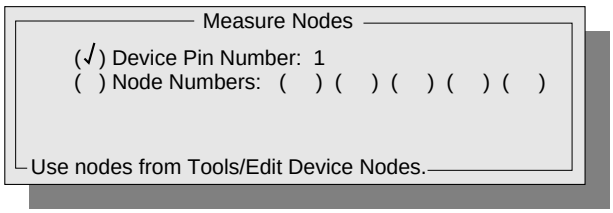
1. From page 2 of the transistor Test Properties, select **Tools/Add Page**.
   The new test page opens. The Test Properties Current Page is 3 of 3.
2. Click **Beta** for the Test Type.
   Look at the data sheet for 2N2222A transistor. Note the Gain and Collector Current.
3. Type **100** as the minimum in the Gain field.
4. Click **NPN** for the Transistor field.
5. Type **150** in the Collector Current field.
6. Ensure that the Scale Field is **ma** (amps).

Enter the stimulus node for emitter:

1. Click the **Emitter** field, and the Stimulus Nodes pop-up window opens.
2. Click between the parentheses left of Device Pin Number to select it.
3. Type **2** in the Device Pin Number field.
4. Click outside the Stimulus Nodes window to close it.

Enter the measure node for base:

1. Click in the **Base** field and the Measure Nodes window opens.



2. Click Device Pin Number to select it.
3. Type **1** in the Device Pin Number field.
4. Click outside the Measure Nodes window to close it.

Enter the stimulus node for collector.

1. Click the **Collector** field.
2. Click Device Pin Number to select it.
3. Type **3** in the Device Pin Number field.
4. Close the Stimulus Nodes box.
5. If you are at a tester, click **Start** to run the test.
6. Click **Save** from the menu bar.
7. Click **Quit** until you return to the Edit menu bar.

Notes on Semi Tests

- For zeners, you must know the anode, cathode, and zener voltage.
- For diodes and zeners enter the anode first, then the cathode node.
- For verification of Semi tests, you must change the Stim Node On field manually.
- For diode and zener tests, if you use Tools/Swap Poles to swap nodes or pins between the Stim and Meas fields, you must edit the Stim Node On field in order to maintain correct polarity of test stimulus.

PwrOff: Analog Power-Off Tests

In this part of the tutorial you will use the longhand mode to create a template to measure across a resistor divider.

Tutorial References

Refer to the **Z1800-Series Component Test Reference**, Chapter 5, for information on analog test techniques

Refer to the **Z1800-Series Component Test Reference**, Chapter 8, for information on templates

The **Z1800-Series Component Test Reference**, for information on longhand tests

Exercise: Create a template to measure across a resistor divider.

To edit the Component Properties portion of the Step Worksheet:

1. From the Main menu bar, click Edit.
2. Click **PwrOff**.
3. Click **Analog** and the analog Component Select window opens.
4. Click **Add** and the Component Properties portion of the Step Worksheet opens.
5. Type **R22-R26** in the ID field.
6. Type **ResDiv** in the Name field.

   This Name becomes the template name in the library; it cannot have any spaces before, after, or within it.
7. Type **Resistor divider template** in the Desc field.

   Do not change the default, Analog Template, in Device Type.

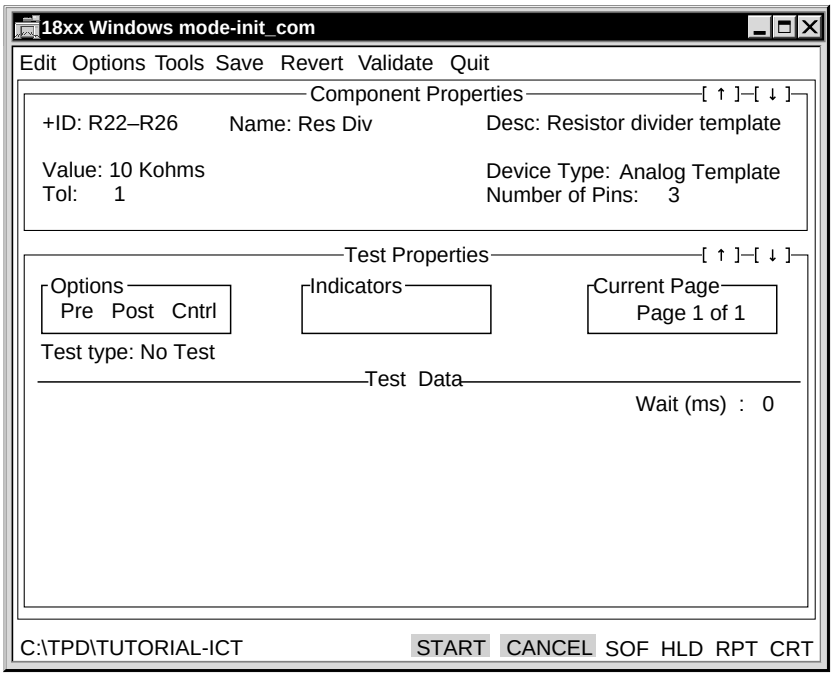
Enter pin data:

1. Type **3** in Number of Pins field and click it.

   The Node Entry window opens.
2. Type **11** for Pin 1.
3. Type **84** for Pin 2.
4. Type **0** for Pin 3.
5. Click outside the window to close it.
6. Click **Save**.

To edit the Test Properties portion of the Step Worksheet:

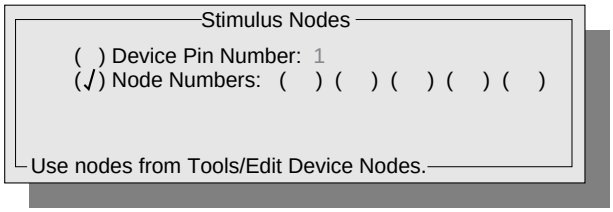
1. Select **Tools/Generate Test**.
   A message appears providing information about the EXCEPT.LST file.
2. Click **OK** to continue.
   Test Properties opens below the Component Properties portion of the Step Worksheet.



3. From the Test Type pop-up list, click **Test V Stim V**.
4. From the **Scale** pop-up list, click **V**.
5. Type **90** in the High field.
6. Type **70** in the Low field.
   Do not change the default, DC, in Measure Type.
7. Type **5.0** in the Stim Value field.
8. From the **Scale** pop-up list, click **V**.
   Do not change the default, DC, in Stim Type.
9. From the **Resistor** pop-up list, click **100 O**.

Enter data in Stimulus field:

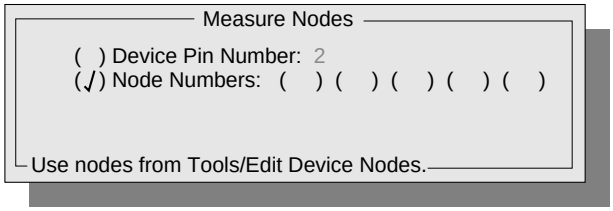
1. Click the **Stimulus** field and the Stimulus Nodes window opens.



2 Click **Device Pin Number** to select it.
Do not change the default Device Pin number.
3 Click outside the Stimulus Node window to close it.

Enter data in the Measure field:

1 Click in the **Measure** field and the Measure Nodes window opens.



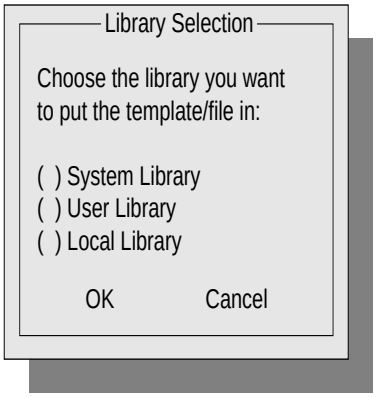
2 Click **Device Pin Number** to select it.
Do not change the default Device Pin Number.
3 Click outside the Measure Nodes window to close it.

Enter data in the Reference field:

1 Click in the **Reference** field and the Guard Nodes window opens.
2 Click **Device Pin Number** to select it.
Do not change the default Device Pin Number.
3 Click outside the Guard Nodes window to close it.
4 Click **Save**.
5 If you are at a tester, click **Start** to run the test.

To create a template:

1 Select **Tools/Create Template**.
2 When prompted, click **Yes** to create a template for the device ResDiv**.**
The Library Selection window opens.



3 Click **System Library.**
4 Click **OK** to store the template in your system library for future use.
5 Click **Quit** until you return to the Edit menu bar.

MultiScan: WaveScan, FrameScan, DeltaScan

Fast Mode is available for WaveScan and FrameScan on Test Properties portion of the Step Worksheet.

Refer to the **Z1800-Series Component Test Reference**, Chapter 5, for additional information about Fast Mode.

Refer to the **Z1800-Series MultiScan User's Guide** for detailed information about using WaveScan, FrameScan, and DeltaScan to perform power-off tests for digital devices.

Board Power

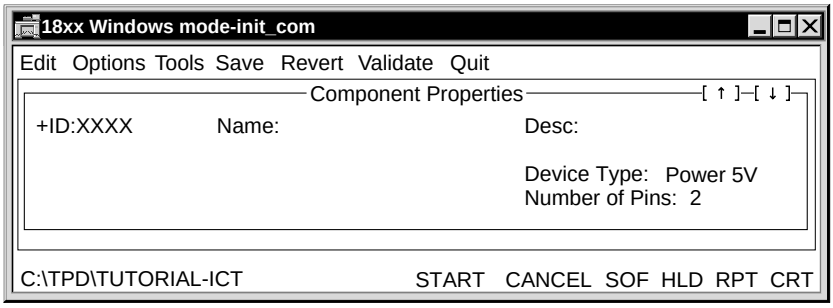
In this part of the tutorial you will add a test for a 5 volt power supply.

Refer to the **Z1800-Series Component Test Reference** for Board Power Test Steps.

Exercise: Create a Board Power test step for 5 volts.

To edit the Component Properties portion of the Step Worksheet:

1. From the Main menu bar, click **Edit**.
2. Click **Brd_Power**.
3. Click **Add**, and the Component Properties portion of the Step Worksheet opens.



4. Type **5 volts** in the ID field.
5. Type **Vcc** in the Name field.
6. Type **Check 5** volts in the Description field.

   Do not change the default, Power 5V, in Device Type.

Enter pin data:

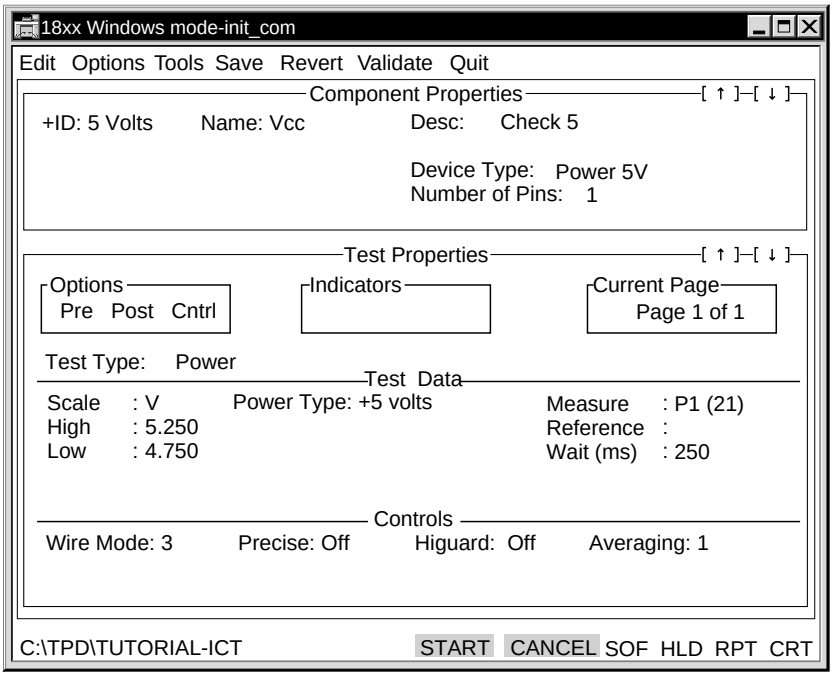
1. Type **1** in the Number of Pins field.

   Power supplies normally have a power pin and a reference pin. The selftest fixture is a special case in that it references the DUT power supply to system ground via the backplane minus pins of the fixture interface. Therefore, the 5V Test Properties in this tutorial does not require a reference pin or node.
2. Click in the **Number of Pins** field, and the Node Entry box opens.
3. Type **21** for Pin 1.
4. Click outside the window to close it.
5. Click **Save** to add the test step.

To edit the Test Properties portion of the Step Worksheet:

1 Select **Tools/Generate Test**.

Test Properties opens below the Component Properties portion of the Step Worksheet.



2 The Test Type field default is Power. T

This test turns on the power supply, and closes all relays to bring voltage to the fixture interface.

3 When Tools/Generate Test is used with the Device Type Power 5V, the system generates a tolerance of 5%. Do not change the default.

4 Do not change the default Wait of 250 milliseconds. .

5 Click **Save**.

6 If you are at a tester, click **Start** to run the test. You should hear the power relays close.

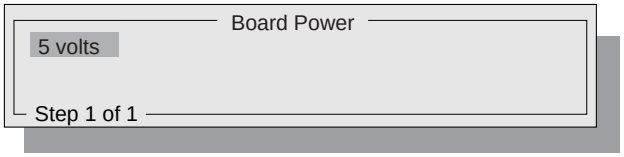
Add a 12 Volt Power Supply

Next you can add a 12 volt power supply to the Board Power test.

Exercise: Adding a 12 volt power supply to the Board Power test.

To edit the Component Properties portion of the Step Worksheet:

1 Click **Quit** to return to the Board Power Component Select window.



2 Click **Add**.

3 To select the location of the new component, click **5 volts**. The new component is added to the right of it, and the Component Properties portion of the Step Worksheet opens.

4 Type **12 volts** in the ID field.
5 Type **+/- Vee** in the Name field.
6 Type **Enable +/- 12 volts** in the Desc field.
7 From the Device Type list, click **Fixed/Slaved PS A**.

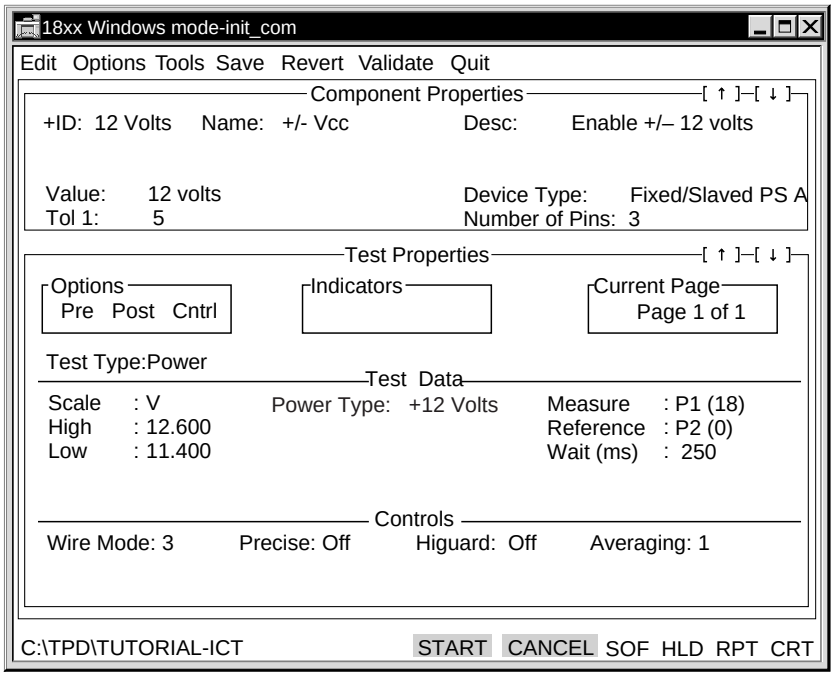
Enter pin data:

1 Type **3** in the Number of Pins field. Then click the field to open the Node Entry box.
2 Type **18** for Pin 1.
3 Type **0** for Pin 2.
4 Type **26** for Pin 3.
5 Click outside the Node Entry box to close it.
6 Type **12** in the Value field.
7 Type **5** in the Tol field.
8 Click **Save** from the menu bar.

To edit the Test Properties portion of the Step Worksheet:

1 From the menu bar, select **Tools/Generate Test**.

The +12 volt Test Properties page opens below the Component Properties portion of the Step Worksheet.



2 From the menu bar, select **Tools/Add Page**.

The Current Page 2 of 2.

3 From the Test Type pop-up list, click **Test V**.
4 Type **-11.4** in the High field.

You are checking negative voltage, so the high field should be less negative than the low field.

5 Type **-12.6** in the Low field.

Enter data in the Measure field:

1 Click in the **Measure** field and the Measure Nodes box opens.
2 Click **Device Pin Number** to select it.
3 Type **3** in the Device Pin Number field.
4 Click outside the Measure Nodes box to close it.

Enter data in the Reference field:

1 Click the **Reference** field, and the Guard Nodes box opens.
2 Click **Device Pin Number**.
3 Change the Device Pin Number to **2**.
4 Click outside the Guard Nodes box to close it.

If you are at a tester, you can:

1 Click **Save**.
2 If you are at a tester, click **Start** to run the test.
The two-page test checks both + and - Vee ±12.
3 Click **Quit** to return to the Edit menu bar.

Notes on Board Power Tests

Board power tests include:

- Power 5V
- Programmable Supply A
- Programmable Supply B
- Power Bus
- Fixed/Slaved Supply A
- Fixed/Slaved Supply B
- PB
- Analog Template.

When you click Power in the Test Type field, the Power Type field opens in the Test Data area of Test Properties. Power Type choices include:

- +5
- +12
- -12
- +15
- -15
- A Adjustable
- B Adjustable
- Measure Only.

The dual V_{ee} supply provides ±12 or ±15 volts to the fixture at the fixture interface pins labeled DUT +V_{ee}, DUT Com, and DUT -V_{ee}. When you click either +12 or -12 in the Power Type field of Test Properties, both supplies will come on, yielding +12 and -12 volts. The same is true if you choose +15 or -15.

The A Adjustable and B Adjustable power types provide voltages to the interface pins labeled PS1 and PS2 respectively. By using multiple pages in Test Properties or multiple test steps, you can generate various supply voltages to the DUT from 0 to 55 volts.

You need two test steps to adequately program the three power supplies: one for +5, and one for the pair of 12/15/Adjustable supplies. The latter test step is a two-page test, one for $+V_{ee}$ and the other for $-V_{ee}$.

During test verification, you can add extra Measure Only steps using the Test V type to test regulators in the fixture, voltage converters, or other bias points in the board under test.

Linear: Op Amps, Voltage Regulators, Comparators, and Relays

Devices in the Linear category may include

- Operational amplifiers
- Voltage regulators
- Comparators
- Relays

You can use a linear test to take voltage measurements. However, since there are no linear devices in the library. you must create the test in the Linear section. For a linear test, the Device Type field in the Component Properties portion of the Step Worksheet is always Analog Template.You can build an analog library over a period of time by using Tools/Create Template to put linear or other analog template tests into the library.

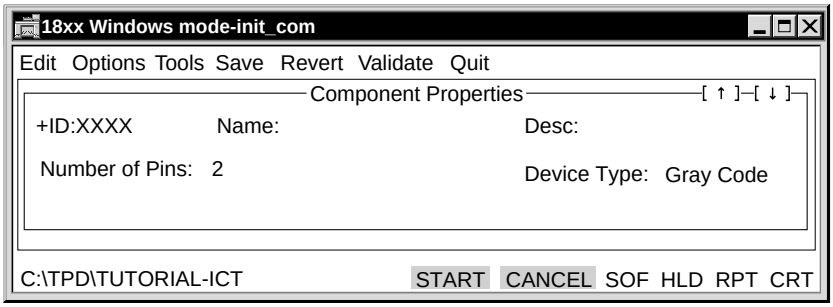
Digital: Gray Code and Vector

Digital IC tests are generated from a library of templates. A template is a test without the node numbers filled in.

If you have an analog-only test system, information regarding digital test is not pertinent to your test situation. The analog-only functionality prevents you from generating, editing, or running digital tests.

Exercise: Creating a Gray code test:

1. From the Main menu bar, click **Edit**.
2. Click **Digital**.
3. Click **Components** and the Digital Component Select window opens.
4. Click **Add**. The Component Properties portion of the Step Worksheet opens.



5. Type **BUS_CHK** in the ID field.
6. Type **DR_BUS** in the Name field.
   This entry is used to search for a template test in the library.
7. Type **Sample check of tied nodes using digital drivers** in the Desc field.

8 Gray Code opens by default in the Device Type field. The number of pins in the Number of Pins field is 2.

Enter pin data in Number of Pins field:

1 Click **Tools** from the menu bar.

2 Click **Get Template Pins**.

If the chip type is in the library, the Number of Pins field is filled with correct number.

If the chip type is not in the library, enter the number of pins, between 1 and 128, and create the test by hand. For devices with more than 128 pins, use a vector test.

3 Type **8** in the Number of Pins field, then click it to open the Node entry pop-up window.

4 Type **68** in the node number field and press **Enter** to advance the pointer to Pin 2.

5 Type the following so that:
Pin 2 = **84**
Pin 3 = **32**
Pin 4 = **54**
Pin 5 = **64**
Pin 6 = **88**
Pin 7 = **36**
Pin 8 = **50**

If you are at a tester, you can:

1 Press **F9** to open Nodefinder and manually probe the board under test. However, the selftest fixture used in this tutorial is enclosed, and you will not be able to probe it with Nodefinder.

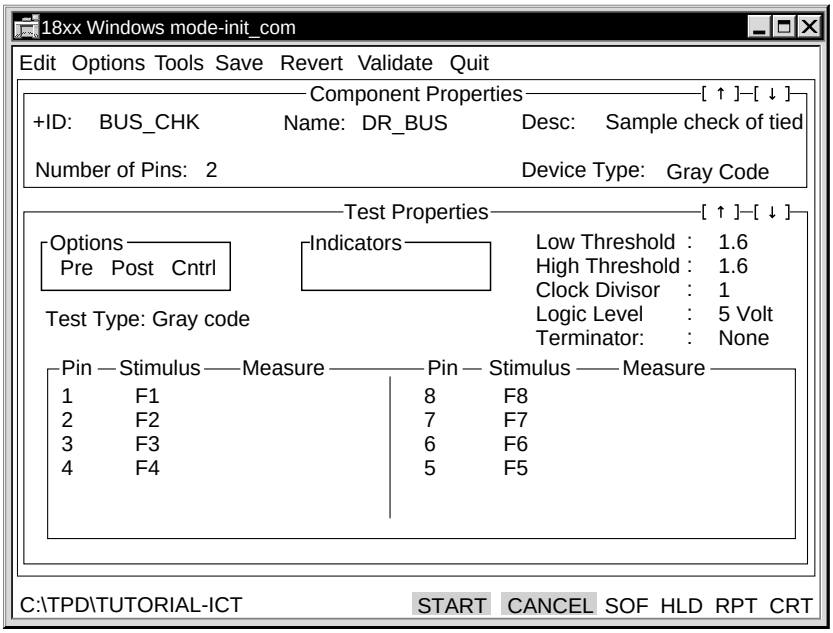
2 Click outside the Node Entry box to return to the Component Properties portion of the Step Worksheet.

3 Click **Save**.

To edit the Test Properties portion of the Step Worksheet:

1. Select **Tools/Generate Test**.
2. Ignore the message and click **OK** to continue.

   The Test Properties page opens showing all eight pins as Stim D Resp D pin type with frequencies F1 to F8.

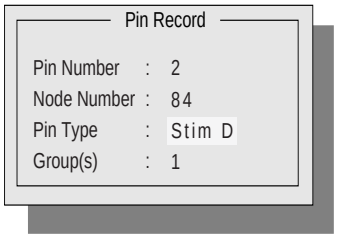


You will change the even-numbered pins of the device to measurement pins.

Enter pin record data:

1. Under Pin, click **2**.

   The Pin Record box opens.

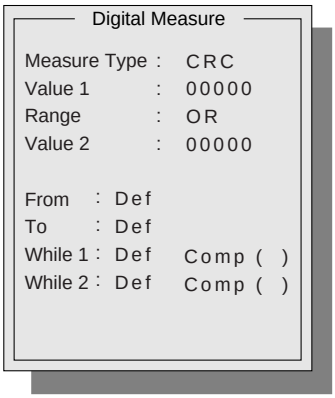


2. Click **Stim D** in the Pin Type field, and a pop-up list of Gray code pin types opens.
3. Click **Resp D** (digital response or measurement pin).
4. Click outside the Pin Record pop-up window to close it.

   The stimulus field for pin 2 closes and CRC 0000 appears in Pin 2 Measure field.

Enter digital measure data.

1. Click **CRC 0000** in the pin 2 measure field, and the Digital Measure box opens.



2. Type **1234** in the Value 1 field.

   You will use the default for the rest of the Digital Measure fields.

   If CRC 1234 is incorrect, you can replace it with the correct signature after you run the test.
3. Click outside the Digital Measure box to close it.
4. Repeat these three steps for pins 4, 6, and 8.

If you are at a tester, you can obtain the correct signatures by running the test. To run the test, you must Enable it for execution. Since the device was not in the library, the system created a default test, but execution was disabled by control options.

Enter Test Step Controls.

1. In the Options box of Test Properties, click **Cntrl**.

   The Test Step Controls box opens.
2. In the Test Page Execution field, click **Enable**.
3. Click outside the Test Step Controls box to close it.
4. Click **Save**.
5. Click **Quit** until you return to the Edit menu bar.

Updating the Component Database

When you finish adding new components, you can update the binary component database.

From the Pgen menu, click **Update**. The component database is created from the information stored in the in-circuit program. The system recreates the component database to include your most recent modifications and a node index.

You can add additional components to the program during test verification, but you must repeat the Update process after each added component.

Verifying Your Test

After you have created tests for all the components, verify your test program to ensure that the program is accurate, stable, and repeatable. Verification takes place in three phases:

- Component level.
- Section level.
- Entire test program.

Verification Tools

You have the following Z1800-series software tools available for test program verification:

- Stop-On-Fail (SOF) and the Stop-On-Fail editor
- Repeat (RPT)
- Hold
- Wait
- Squelch
- Diagnostic Messages
- EXCEPT.LST
- Nodefinder
- Global Validate, in which you can select other tools

Stop On Fail (SOF)

When SOF is selected, the program stops running at a failed test step. You have the option of either continuing the test program or editing the failing test.

You can use SOF during section and global program verifying:

1. Click **SOF**.
2. Click **Yes** to edit the test or click **No** to continue program execution.

   When you click Yes, the Test Properties for the failed component opens, and you can edit the test. You can then test your modifications by clicking Start.
3. Click **Save** when you complete your modifications.

Repeat (RPT)

You can use RPT with SOF to identify intermittent test failures. When RPT is selected, a single measurement outside of tolerance will stop execution and show failing data. RPT is not available for shorts or ignores.

When you click RPT, the test program repeats one measurement. You can either:

- Click Start to forward the program to the next measurement, which will also repeat.
- Click RPT to deselect it and stop the repeat.

If the test step has a single measurement, click Start when RPT is selected and the program continues to the next step. If you are verifying a single page Test Properties, click Start when you repeat the last measurement of a component deselects RPT.

To use RPT:

1. Click **RPT** button to continuously repeat a test.
2. Click **RPT** again to end the cycle.

   Pressing Start advances you to the next measurement which will also repeat.

Use the Repeat Page Option Variables, such as Repeat Delay, Repeat Mode, and Repeat Count, to specify how you want RPT to work. This is useful in situations where there is poor probe contact. The operator can cycle the vacuum while repeating failing tests.

Hold (HLD)

Click HLD to stop the program at each measurement in sequence. You can then test the program measurement by measurement.

Wait

Click Wait to delay the measurement made by the ATB with respect to the stimulus, in individual Test Properties. If necessary, you can increase wait time to allow stimulus to settle or change surrounding circuitry before a measure is strobed.

Squelch

Squelch discharges the measure node for a specified period of time prior to the measurement being taken. In individual tests, you may need to lengthen squelch to allow charges left by previous tests to dissipate.

Refer to the **Z1800-Series Component Test Reference** for more information on Squelch.

Diagnostic Messages

A variety of diagnostic messages or data is shown during test execution. You can customize these messages to provide such information as component name, ID, description, failure data, high/low limits, measure node, pin number.

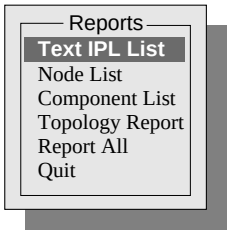
Program Generation Outputs

When you select Pgen/Reports/Report All, program generation results in several outputs, such as:

- **EXCEPT.LST**. Automatically generated in the Pgen-Build process and can be opened through DOS.
- **IPL.LST, NOD.LST, and COMP.LST**. Automatically generated when you select the individual report or Report All.
- **TOPOLOGY.LST**. Automatically generated when select Topology Report from the Reports menu.

You can use Reports to generate information about the nodes, components, input list, and topology for a board test. The reports apply to the active board test directory.

1. From the Main menu bar, click **PGEN**.
2. Click **Reports** to open the following pop-up menu.



- **Text IPL List** generates a text file documenting the contents of the binary component database file, IPL.DBF.

  IPL.LST gets data from the component database. It may differ from your original text input list because of program changes. Update your component database to reflect the latest program changes before you generate IPL.LST.

Do not use IPL.LST as an input for Build to regenerate a program. If you regenerate a complete test program from this file by renaming it to IPL.DAT and doing a Build, you will lose all of your test data such as guard points, test modes, wait times, pre- and post-test option menu settings.

- **Node List** generates a nodes-to-components reference table that describes the board topology sorted by node number and lists all components connected to the nodes.
- **Component List** generates a components-to-nodes reference table that describes the board's topology sorted by component and component pin, listing all connected nodes.
- **Topology Report** generates two report, one lists components with matching IDs but different nodes, the other lists components with different IDs but matching nodes

  Refer to the **Z1800-Series Component Test Reference**, Chapter 7, for detailed information about Topology Report.
- **Report All** generates all of the above lists. These files are located in the board directory.

Using EXCEPT.LST to Analyze Program. As your test program is generated, a number of test status messages appear on your monitor. These messages, stored in EXCEPT.LST, can be helpful to analyze and verify the test. A date and time stamp indicating when the message was written identifies incremental changes made to the program.

Use the DOS shell to open EXCEPT.LST from the board directory.

Global Validate

After you have entered all the components into the program and have verified the fixture wiring, you can use Global Validate to find analog guards and to automatically verify the tests.

Validate improves test measurements by finding guard points of the resistors and capacitors in your program. It determines the correct guards, wait time, squelch time, and polarity of stim/measure. The component database must be current for Validate to work.

Global Validate is available only for resistor, capacitor, and Multiscan tests. The other power-off analog tests require manual verification.

Refer to the **Z1800-Series Component Test Reference**, for information about the Validate Configuration window.

To begin verification:

1. From the Main menu bar, click **Files**.
2. Click **Select**.
3. Click **Tutorial**
4. Press **Enter**.

Header Verification

There are two kinds of Header test steps:

- PRGMVARS (program variables)

  Sets global flags and variables used throughout the test program
- msg (messages)

Verifying the Header ensures that the global settings you selected in PRGMVARS properly control the test execution, in both Debug and Run mode.

The Header provides options for handling and reporting failures.

Tutorial References

The following references are in the **Z1800-Series Component Test Reference**, Chapter 3.

- Information on editing headers
- A listing of PRGMVARS test step choices
- A listing of the Header/Trailer message step

Also refer to:

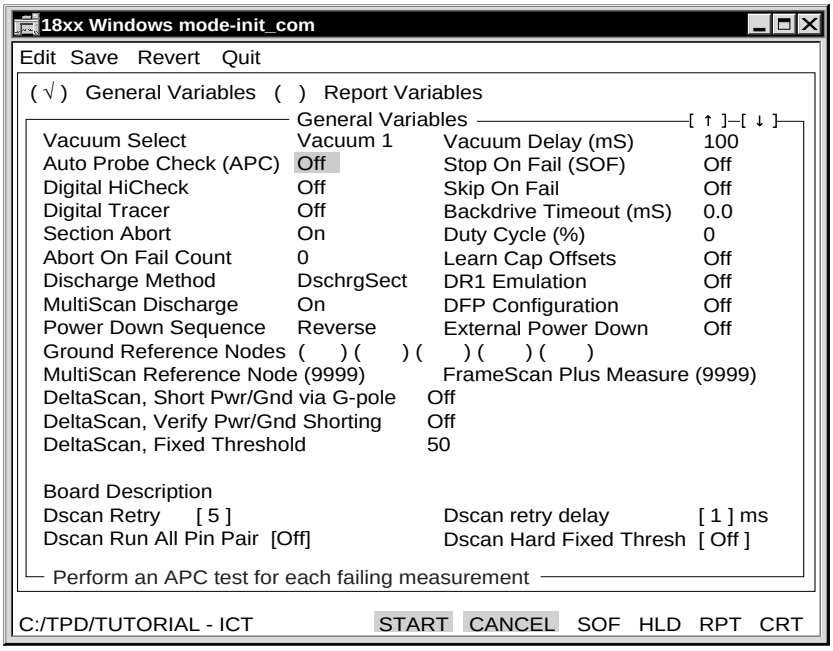
- Notes on Verifying the Header in this chapter, and
- The **Z1800-Series Multiscan User's Guide** for additional information regarding the Learn CapPhase Offsets.

Exercise: Verifying the Header

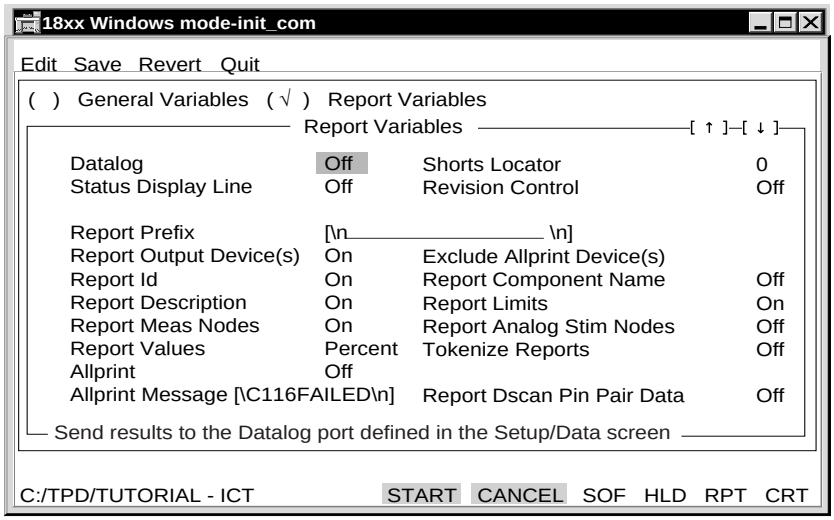
1. Select **Edit/Header**
2. Click **PRGMVARS**.

   PRGMVARS has two main windows similar to the following illustrations.

This is the General Variables window:



This is the Report Variables window.

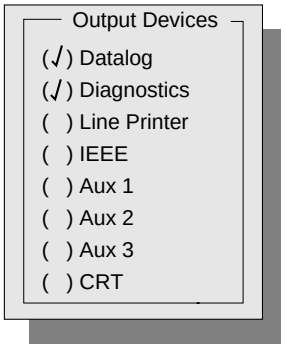


- Click the name of the window you want to open.
- An explanation for selected variable appears in the lower portion of the window.
- Click the up and down arrows to move to additional pages for each window.
- Set a flag by clicking it **On**.

For this tutorial, leave the settings as they appear in the above illustrations.

In regard to Ground Reference Nodes in the General Variables window, normally the board-under-test ground traces are listed here; however, the tutorial selftest fixture has no ground node, so you can leave this field blank.

Verify your selection of output devices by clicking **Report Output Device(s)**. A pop-up list opens where you can select the output channels for failure data.



1. Click **Datalog** to deselect it.
2. Click outside the Output Devices pop-up list to close it.
3. Click **Save** from the menu bar.
4. Click **Quit** until you return to the Edit menu bar.

Auto Probe Check

Auto Probe Check verifies that the fixture pins of a failing component were making good contact when the component failed thus eliminating false failures due to the fixture. Use this function for both verification and production testing.

Digital HiCheck

Digital HiCheck converts all stuck high CRCs to HIGH and all stuck low CRCs to 0000 for easier visual recognition. Gray code tests often report stuck high and stuck low faults as a 4-character hex code. Digital HiCheck is normally used for test verification.

Skip On Fail

Skip On Fail causes the test program to skip remaining measurements on an individual component as soon as one measurement fails. Since you must replace a failing component when one or more elements of a device are defective, Skip On Fail assures board execution time is not wasted. Skip On Fail is normally used in Run mode; however, during test verification, you would turn Skip On Fail off in order to check each element test.

Section Abort

Section Abort prevents failures in interconnections (Intc), such as Shorts, from interfering with subsequent analog measurements. It also prevents the tester from applying power to a board that is known to be defective, that is, has failures in Intc, Passive, Semi, or PwrOff. You can turn Section Abort off while verifying a program on a known good board. Section Abort Off is a verification function only.

Ground Reference Nodes

In the Ground Reference Nodes field, you can enter up to five node numbers that can always be safely connected to the tester's chassis ground when all power supplies are turned on. This field is important in determining how Brd_Power and Linear tests handle voltage measurements.

Interconnections

Interconnect components must be verified in combination with each other, since shorts must be verified last. You must be at a tester to perform the following exercise.

Exercise: Verify interconnections

To test for jumpers:

1. From the Main menu bar click **Edit**.
2. Click **Intc**.
3. Click **Jumpers**.
4. Click **Start** to check test performance.
5. Release the vacuum and click **Start** to make sure the tests reject open circuits.

   Edit each jumper ID and Component ID. If possible, physically remove jumpers on the board to verify proper test and diagnostics.
6. Click **Quit** to return to the Edit menu bar.

To test for continuities

1. From the Edit menu bar, select **Intc/Continuities**.
2. Click **Start** to check the test performance.
3. Release the vacuum and click **Start** again to make sure the test rejects open circuits.

   Normally all continuities are listed under a single test step page.
4. Click **Quit** to return to the Edit menu bar.

To test for special cases

1. From the Edit menu bar, select **Intc/Merge SC**.
2. Click **Start** to check the test performance.
3. Release the vacuum and click **Start** again to make sure the test rejects open circuits.
4. Click **Quit** to return to the Edit menu bar.

To test for shorts

1. From the Edit menu bar, select **Intc/Shorts**.
2. Click **Start** to check test performance.
3. Click **Quit** to return to the Edit menu bar.

   Short two nodes together and use Start to run the shorts test.

If you have jumpers, continuities, and ignores in your Intc section, some pairs of nodes can be connected without causing failures. A clip lead between any single node and any jumper node, continuity, or ignore group will cause a failure.

Analog Components

When verifying analog components, check for repeatability, stability, linearity, and the validity of guards. Program analog component sections for minimum wait and squelch times.

Verification Summary

- Check that the measure pole is on the most isolated side of the component—the side that has the fewest other components attached.
- Try guarding around the measure pole, one component away.
- Use the minimum number of guards after trying all possible guard points.
- Reverse stim/measure polarity on the component, then repeat guarding, if necessary.
- Experiment with wait time.

  Certain circuit configurations may require wait time. For example, a capacitor in the surrounding circuitry needs time to charge so that it will not influence the measurement.
- Try increasing Squelch time if, for example, the measured capacitor has retained some residual charge from a previous test step.

Using Validate to Verify Analog Components

If the test is a FAIL for a resistor or a capacitor, and you have not already run global Validate from the Pgen menu, click **Validate** for a single test step to find guard points that will bring the test results within limits.

Validate uses the component database to find potential guards and to adjust squelch, and waiting stim/measure polarity.

If Validate does not succeed or if the failed component is not a resistor or capacitor, work with the schematic to identify other guard points. The component on your sample board must be good.

Bypassing a Measurement

If you cannot get a good measurement, you can bypass a component and come back to it later.

To bypass a component:

1. From a Step Worksheet Edit menu, select **Options/Controls**.
2. Click **Test Page Execution**.
3. Click **Disable**.
4. Click **Save**.

Swap Stim and Meas Poles

It may be easier to get a satisfactory guard list when the Measure point is not on a power bus. You can reverse Stimulus and Measure pin assignments in the tester by selecting **Tools/Swap Poles** from the Step Worksheet Edit menu. This exchanges the pin numbers (node numbers) in the Stimulus and Measure fields. Validate automatically swaps the Stim and Meas points when searching for potential guards.

Guarding

An unguarded parallel current path around a component causes the tester to report a smaller impedance than the actual impedance. For example, a 1 k resistor may be reported as 500 ohms.

Putting in the guard diverts the parallel current from the measurement path, raising the impedance that the tester sees. A guarding problem does not show up as a too-high impedance reading because guarding is done in a situation where stray (extra) current is erroneously leaking into the measurement, causing a seemingly lower impedance. If the tester is reporting 2 k for a 1 k resistor, then the problem is not a guarding problem. You may have a wrong part on the sample board, or a defect in the fixture.

Use Test Jacks

You can use the test jacks during analog verification. Some THC boards have 100 Ohm resistor in series between the testhead jacks and the E, F, G bus. Consider these resistors when you connect components in parallel via these test jacks.

If the test jacks poles and triggers are enabled from Setup/System Variables, you can:

- Use the E pole, which is useful for verifying capacitor tests.

  If the signal does not look like a sine wave, the test is probably ineffective. Connect an oscilloscope input to the E (stimulus) jack. The F (measurement) jack is a virtual ground for guarding that may change ground if you suspect that the measurement amplifier is saturating. Trigger the oscilloscope from the Test Envelope jack, and also observe the Listen Window signal. The Test Envelope signal, normally high, goes low for the duration of the test sequence. The normally low Listen Window pulse (the pulse is low or the base level of the signal is low with a high pulse) marks the analog-to-digital conversion.
- Connect from E to F a decade box of the same type of component you are verifying. If you are verifying a resistor test, use a resistance decade box.

  If you set the decade box to ten times the impedance value of the component you are measuring, the tester should report a 9% lower impedance value. For example, a 100 kohm resistor added in parallel with a perfect 10 kohm resistor under test should cause the tester to read 9.091 kohm. A 1000-picofarad capacitor added in parallel with a perfect 10-nanofarad capacitor under test should read 11 nanofarads.

Reverifying Power Wiring

You should check power wiring before applying power to the board and proceeding with the verification procedure.

- Make sure that the power supplies are grounded correctly.
- Make sure wiring from multiple power supplies doesn’t conflict.

If optional programmable relays are involved, use clip leads to simulate their contacts, and buzz out the connections to verify no shorts will occur on power up.

Board Power

Before powering up, check the programming of the board power test steps. Check for correct voltages, reasonable measurement limits, and that the failure messages are not misleading. If multiple power supplies are involved, check for correct sequencing of power up.

To check the board power test steps:

1. From the Main menu bar click **Edit**.
2. Click **Brd_Power**.

   The Board Power Component Select window opens listing the 5 Volt test you created earlier in the tutorial.
3. With 5 Volt selected, click **Start** to turn on power and execute the entire test section.

   The status bar shows measurements.
4. Click **Quit** to return to the Edit menu bar.

Board Power Verification

Incorrect wiring is a common cause of board power failure. You can use Nodefinder to help verify that all nodes are correctly wired to the respective power and ground planes. Nodefinder does not ensure that power wires from the available user source supplies are correctly wired. Along with the current carrying wires, the sense wires (one for drive and one for return) must be properly wired or the board power test will fail.

If the tester tries to turn on either A or B Adjustable supplies when voltage is not adjusted correctly, the A or B tests run in repeat, and the following message and measured value appear:

```
Running ICT Test Program NNNN adjust supply A to requested value, then press START
Testing in progress. . .
High:15.750  Meas: 17.948  Low:14.250 V  Node: 2  . .
```

1. Adjust the supply until the appropriate voltage is listed in the Meas window.
2. Press **Start** to continue verification.

After verifying the Brd_Power test, reverify the board power. Refer to page 36 for more information about Reverifying Power Wiring which immediately precedes this section.

Press **Cancel** at any time during verification to turn off all power supplies.

Linear Components

Verify a test for linear components by checking that:

- All associated power rails powered up.
- The nodes in the Reference field are differential or grounded.

  If the test requires the node to be grounded, the node must be listed in the Header. You can have up to five safe Ground (GND) nodes in the Header.
- The nodes in the correct locations.

You can:

- Check Stim values by performing Stim and Measure at the same node.
- Check the specifications of the analog test board (ATB) and work within those limitations.

Test V and Test V Stim V

Test V and Test V Stim V are the available Linear tests. Test V is a measure-only test step—there is no stimulus. Test V Stim V provides a stimulus voltage through a selectable series resistor, measuring the same way Test V measures.

The voltage measurement is either single-ended or differential, depending on what you select in

the PRGMVARS Ground Reference Nodes field and what you program into the Test Properties Reference Node field.

Ground. For Test V and Test V Stim V tests, the ATB always references system ground. One side of the measurement system hardware is internally hardwired to system ground. The DUT power supplies are also referenced to system ground. When DUT power is on the board-under-test, placing the reference side of the ATB on various nodes indiscriminately may damage the board and/or system.

When you wire the fixture, remember that the system ground (ATB ground) presents itself in the fixture at the GND (REF) pin. Therefore, the board-under-test ground and any power supply grounds connected to this point become system ground, too.

Any nodes connected to this point should be listed in the Header/PRGMVARS Ground Reference Nodes field. If you list these nodes, then any power on Linear test steps will be protected from switching any other nodes on the board to system ground.

When there is a ground reference conflict, the measurement will be made using a differential type of measurement. You can request voltage measurement/reference points anywhere on the board without having to worry about safe grounds. The system indicates a differential measurement by prefacing the measured data with a D character.

	Header Ground Reference Nodes	Test step Reference Nodes	Measure type	Nodes at System ground
A	(blank)	(blank)	Standard	(none)
B	237	(blank)	Standard	(none)
C	(blank)	237	Standard	237
D	128	128	Standard	128
E	238	237	Differential	(none)

A. The Ground Reference Nodes field in the Header/PRGMVARS step is blank. The Reference field in the Step Worksheet in the Linear category of the test program is also blank. Only a measure node is specified. In this case, standard measurement is made between system ground and the measure node.

B. Node 237 is not used at all. It is listed as safe to ground, but no request to ground it comes from the test step because the Step Worksheet has a blank Reference field. Therefore, the measurement is made from system ground to the requested measure node.

C. Node 237, the reference node in the test step, is used. It is switched to system ground potential since no conflict with the Header/PRGMVARS Ground Reference Nodes field exists.

D. Any node entered in both the Header Ground Reference Nodes field and the Test Properties Reference field will be added to system ground. Test Properties requests node 128, and the Header confirms that 128 is safe to ground.

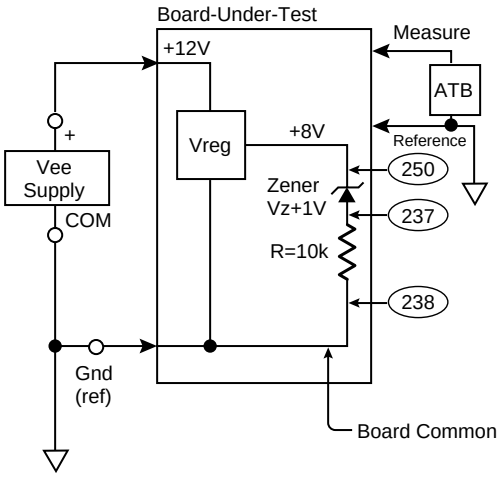
E. Node 238 is listed as **safe to ground** in the Header/PRGMVARS Ground Reference Nodes field.

The system uses a differential measurement to avoid a grounding problem that could cause damage to the ground and the zener by overcurrent. In the drawing below and **E** above, assume measurement of the voltage across the zener. When the test step requests 250 as the measure node and 237 as a reference, the system finds that 237 is not in the Ground Reference Nodes list; therefore, it cannot be safely switched to ground.

The system measures the voltage from system ground to node 237. Then it measures from system ground to the requested measure node, node 250. It subtracts the voltage at node 237 from the voltage found at node 250. The result represents the voltage at mode 250 relative to the voltage at node 237.

A D character precedes the data to indicate a differential measurement. Node 238 was not used in the measurement, but was noted as a listed **safe ground** point. The ground connection is through the internal system ground and GND (REF).

The following illustration is a dialog example showing differential measurement application:



WARNING!

Connecting both nodes in the Ref Node field, as stated in the following paragraph, is a great convenience for testing certain comparators and amplifier ICs; however, it requires programming caution. In Linear, the tester will not prevent programming a switch setup that may damage the tester. For example, node 0 is ground and node 1 is Vcc. Node 0 is declared in the Header/PRGMVARS page—the tester regards it as a safe ground point. Programming a Linear test with both 0 and 1 in the Ref Node field closes G relays on node 0 and node 1 across the supply, destroying the relays and possibly fusing other circuits as well.

If the Linear test page's Reference field contains two node numbers and one of them is the same as the safe ground node declared in the PRGMVARS page, then a single-ended measurement is made. Both of the nodes in the Reference field are connected to chassis ground through the G-pole reed relays. You can use this feature to get an extra zero-volt stimulus.

Digital Tests

Many devices with linear functions can be tested as digital devices wherever stimulus voltages can be 0 and 5 volts, and response voltages between -2 and +10 volts. Such devices include field effect transistors, relays with 5-volt coils, and the majority of op amp and comparator configurations.

Other devices such as digital-to-analog (D/A) converters can be tested using mixed analog and digital tests. These mixed-mode tests are part of digital test steps. Build tests for devices that fit these criteria using digital techniques.

Refer to **Z1800-Series Component Test Reference** for more information about mixed-mode tests.

Devices that do not fit these requirements can be dealt with as Linear tests.

Goal

The main goal of a digital in-circuit test is to check connections between the board and the pins of the chip under test. To verify the ability of the stimuli to reveal open input pins, change the stimuli one at a time, ensuring that each change in stimulus causes at least one signature to change.

WARNING! If you apply a power supply that is outside the rail of the driver to a digital driver and press Start, damage occurs to the driver for the connected node.

To change a stimulus without changing the length of the default listen window, change the node number instead of changing the Gray code specification.

If you can change an input pin's stimulus without causing any output signature to change, the test may be unable to detect an open connection on that input pin.

Precedence of Digital Pin Activity

If more than one type of digital activity (stim/meas, guard, or disable) is assigned to the same node during any particular device test, only one of these digital activities occur. The order of preference selects stim/meas activity over guard activity, over disable activity.

Exclusive selection order is:

- Stim/meas activity
- Guard activity
- Disable activity

In addition, if the same digital pin activity type (stim/meas, guard, or disable) is assigned in both Gray code and vector environments during any particular device test, the one matching the current device test type prevails. For example, if a Gray code guard and a vector guard exist on the same node during a Gray code test, the Gray code guard will prevail.

Selection order for Gray code tests:

- Gray code stim/meas
- Gray code guard
- Vector guard
- Gray code disable
- Vector disable

Selection order for Vector tests:

- Vector stim/meas
- Vector guard
- Vector disable
- Gray code disable

Gray code guard is undefined in vector tests.

Adding a Gray Code Disable

The disable table lists stimuli that apply to all digital tests. The program generator analysis produces the disable table entries from template library information to force the outputs of tristate devices into high impedance states.

Stimuli can be added to the list for devices that are not in the program generator library or that are entered into the program by hand. The information you type into the disable table causes the

system to disable data buses on the board under test in such a way that no bus activity exists to disturb other in-circuit (IC) tests.

Where a stimulus programmed in an individual test conflicts with one programmed in the disable table, the individual test program takes precedence over the disable table.

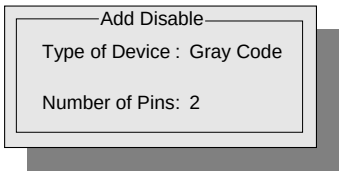
The F2 key does not apply to the Disable Test Properties.

Exercise: Editing the Disable Table

In order to do this exercise, first you must add a disable.

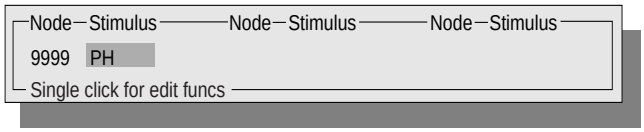
Once you have applied power:

1. From the Main menu bar, click **Edit**.
2. Click **Digital**.
3. Click **Disables** and the Disables Component Select window opens.
4. Click **Add** and the Add Disable window opens.



5. Do not change the default Gray Code as the Type of Device.

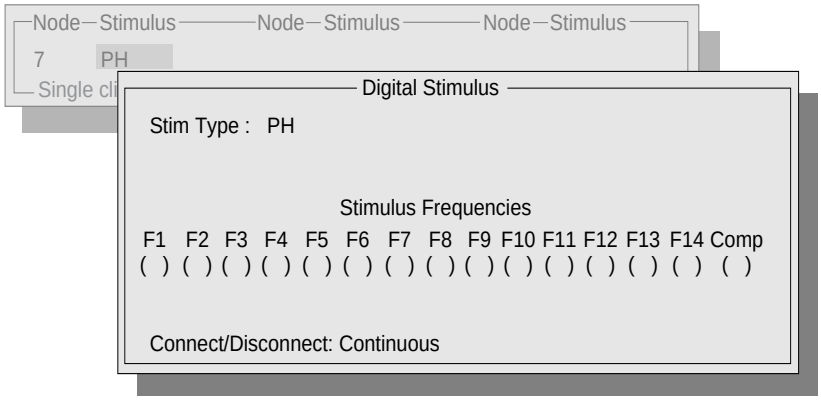
   If a Gray code disable already exists, an error message opens, and you are returned to the Component Select window.
6. Type **1** in Number of Pins.
7. Click outside the Add Disable box, and the Disable Table opens.



To edit the Disable Table:

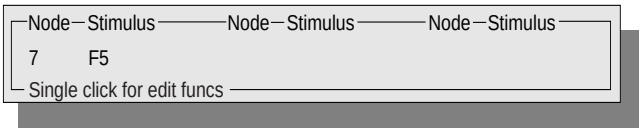
1. Move the pointer to **9999**.
2. Type **7**.
3. Click under **Stimulus**.

The Digital Stimulus pop-up window, similar to the one shown below, opens.



4. Click the **Stim Type** field and pop-up list of stim types opens.
5. Click **Freq**.
6. Click between the parentheses under **F5** to select it.
7. Click outside the Digital Stimulus window to close it.

   The Disable Table shows your modifications.



To add a disable:

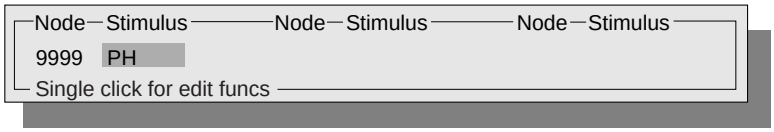
1. In the Disable Table, click **7**, and the Disable Commands pop-up window opens.
2. Click **Add Disable**.
3. On the menu bar, click **Quit**.
4. When prompted, click **Yes** to save your edits and open the Disables Component Select window.
5. Click **Quit** to return to the Edit menu bar.

Edit Gray Code Guards

Gray code guards are similar to disables in that they prevent interference with component tests. A digital guard is active only during the test step in which it is programmed, whereas disables are opened on every digital test step.

Exercise: Edit the Gray code guards for a test

1. From the Main menu bar, click **Edit**.
2. Click **Digital**.
3. Click **Components**.
4. From the Component Select window, click **Bus_Chk** and Component Properties and Test Properties open.
5. From the menu bar, click **Edit**.
6. Click **Gray Code Guards** and the Node/Stimulus window opens in the Test Properties.



7. Click **9999**, and a pop-up window opens with the option to Add or Delete Guard.
8. Click **Add Guard** and close the window.
9. Click **Save**.
10. Click **Quit** until you return to the Edit menu bar.

Disable Digital Buses

You can add tests to see that the settings you made in the disable tables are disabling the digital buses. The stuck bus tests should be the first digital test steps in your program so your program can skip to the end on failure without printing other false failures.

A test for a stuck bus involves two steps:

- Tests whether a small current can pull the bus high, and
- Tests whether a small current can pull the bus low.

If this limited current can indeed drive the bus, it means that all other devices on the bus are properly disabled. The current in both cases is supplied by the tester's terminating resistors programmed in the Test Properties of the stuck bus test.

Different buses require different amounts of current. For example, if there are terminating networks already in place on the board-under-test, the tester's terminators cannot move the bus through a full logic swing, and thresholds need to be reprogrammed or different tester terminators selected.

Examples of stuck-bus tests are given in the Demo program. You can add Bus 1 and Bus 2 tests, or modified versions of them, from the Demo program to your own library. Add them to your test by including input list lines that call them from the program generator, or add them as you would any templated test.

Running the Test

To examine all the signatures, press Hold (F6) or Repeat (F7) before selecting Start. Repeat constantly refreshes the results of each burst while the burst is repeated. Intermittent failures show as blinking highlights. To advance to the next burst, press Start (F3).

Test Properties may have more than one burst. The results of each burst are shown in the measurement window. Failing signatures are highlighted.

The Z1800-series tester can take up to six measurements simultaneously in one burst if both the program and fixture wiring configuration permit. The software system makes decisions about

routing and resource allocation without programmer intervention. The measurement window reports the results of one burst at a time; you can quickly find a particular result by advancing to the burst where it is shown.

Test Jacks in Digital Test

Refer to the **Z1800-Series Component Test Reference**, Chapter 9, for Using the Test Jack Panel in Debug.

If the test jacks are on, you can investigate a burst by examining signals at the test jack panel. Trigger your oscilloscope or logic analyzer using the Test Envelope and/or Listen Window jacks.

For a Gray code test, the Test Envelope goes low when backdrive signals are applied, and returns to high after the last clock in the burst. The Listen Window is normally low but goes high only while signatures are being recorded within the Test Envelope.

For a vector test, the Test Envelope extends from the first state of the vector through the last state. The Listen Window is high whenever an Up or Down is expected on the pin assigned to the E Pole by default. The only way to assign the Listen Window to another pin is to select the Trigger function in the Pin Record Menu of the appropriate pin.

E, F, G, Es, Fs and Gs jacks are connected to the outputs of the comparators that are listening during the burst. The receivers on the driver/receiver boards compare measured signals to the threshold limit. The test jack panel signals are the result of this threshold comparison.

Depending on the matrix allocations, up to six signatures can be taken at once in a single threshold test. The six result signatures shown during a burst are, from left to right, the signatures of the data at the E, F, G, Es, Fs, and Gs jacks, respectively.

Dashes (-) indicate the pole was not used during the burst, either because of an allocation limit or because of the Digital Group combine/separate flag.

When you use dual threshold tests, only three signatures can be taken per burst. Each signature is composed of signals on two of the jacks. Automatic matrix allocation routines determine which node feeds each jack. In dual threshold tests, the two signals at the test jacks should be identical. Differences between the high and low threshold comparisons indicate a bad device or threshold problem.

Gray Code Group Control

Each pin in a Gray code test belongs to one or more groups. A group is an independent part (logic element) of the IC, for example, one inverter in a hex inverter. A pin that is part of all the elements of an IC, for example, a common enable to an octal bus buffer, must belong to all the groups in its digital test step. If possible, the tester will test all the groups in one burst. This is not possible when a test for one group has a different listen window (measure timing) from that of another group.

If the Gray Code Groups flag is set to Separate, each group gets a separate burst whether the groups have common listen windows or not. If the Gray Code Groups flag is set to Combine, the software system attempts to run more than one group per burst.

Guarding

If a test does not pass and you know the sample board is good, then verification is primarily a matter of electrically isolating (digital guarding) the device and finding the correct stimuli and learning the output signatures.

Choosing and Fault-Grading Gray Code Stimuli

Typically, higher frequencies (F1, F2…) are used on clock pins. Lower frequencies (…F13, F14) are used on major mode controls. Middle frequencies are used on address and data pins. The

signatures you receive depend on the IC functionality and stimuli assignments.

Learning and Fault-Grading CRC Signature

A signature test of an output is capable of detecting a pin fault if the pin is high during part of the burst and low during another part of the burst. In the test program it is preferable to see signatures representing a pattern other than a constant low or constant high level.

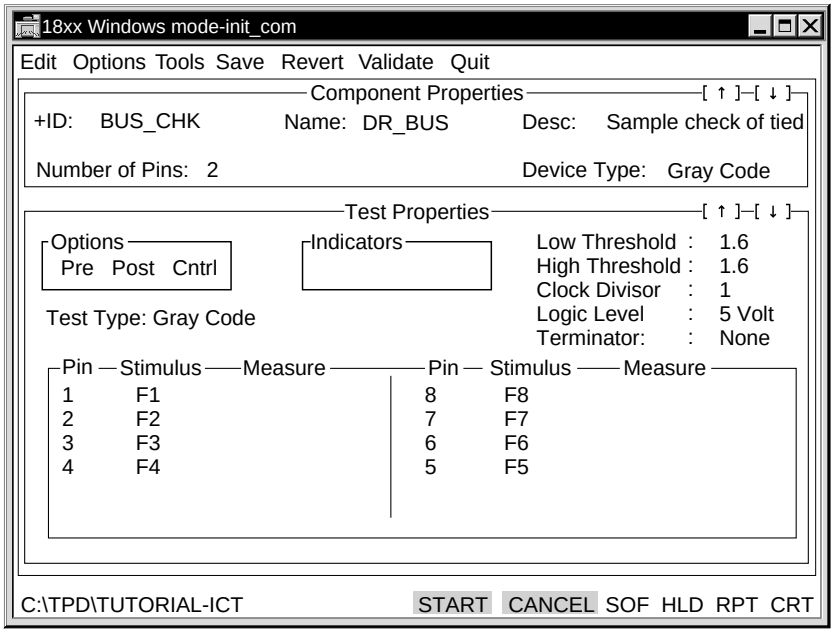
The CRC signature of a pin that is always low is 0000. The CRC signature of a pin that is always high varies according to the number of clock cycles in the Listen Window.

The tester's HiCheck feature identifies signatures of constant high signals automatically. The signature of a failing constant-high node is reported as High instead of the normal 16-bit signature word. You can program the HiCheck feature in the Header/PRGMVARS page. HiCheck does not report High for a signal that the program expects to be high, so you should examine the signatures before learning them.

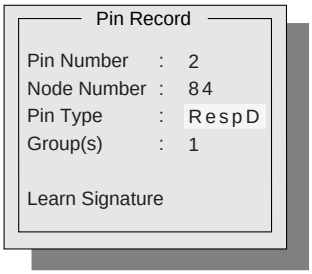
Exercise: Learn the CRC signature of a pin.

To learn the signature and thus convert it to a high:

1. From the Main menu bar, select **Edit/Digital/Components**.
2. Click **Bus_Chk** in the Digital Component Select window.



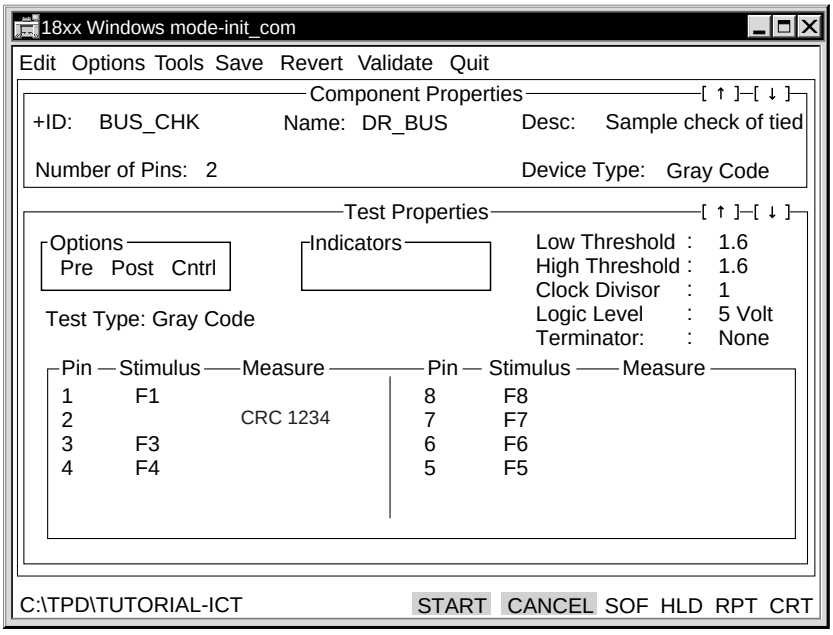
3 In the Test Properties portion of the Step Worksheet, click **2** in the Pin field. The Pin Record window opens.



The Pin Record contains a Learn Signature field that is created when you first run a test for Response and Stim/Response pins. Selecting Learn Signature writes the signature into the Value 1 field in the Digital Measure pop-up window.

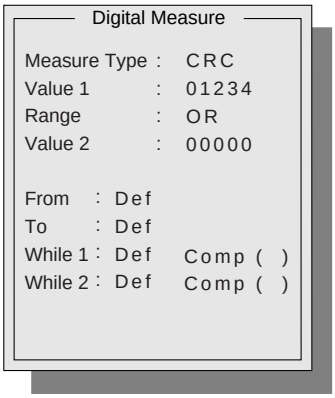
1 Click **Learn Signature** in the Pin Record window.

The Pin Record window closes. The Measure field in Test Properties now contains CRC 1234.



2 Click the **Measure** field for Pin 2. The Digital Measure window opens, where the Value 1

field shows 01234, the signature of the CRC.



3. Close the Digital Measure window.
4. Click **Save** from the menu bar.
5. Click **Quit** until you return to the Main menu bar.

If any outputs of an IC are either High or 0000, the IC is not being stimulated with the right patterns to make the outputs move. If an output doesn't move during a burst, then the tester may not be able to tell whether it is open. If none of the outputs move, then open inputs will not be detected.

If you have tried all reasonable combinations of Gray codes on the inputs without getting activity on the outputs, check the outputs statically. Use the tester's Terminators to apply resistive loads to the outputs of the device. One step can pull up against low outputs, and another pull down against high outputs. If an output pin is not soldered, one of the bursts will fail. This method often enables the tester to perform presence and orientation tests on deeply sequential ICs that are not traditional Gray code targets.

Stabilizing Signature

Counters and flip-flops, especially in S and LS families, sometimes require extra care to stabilize. The tester's rise times are designed to be slow to prevent overshoot at the ends of unterminated fixture leads. As a result, the counter's clock input spends a few extra nanoseconds passing through its transition region. Double counting may result if conditions are less than perfect.

Adding digital guards or moving a stimulus back one device to avoid overdriving high current outputs prevents rise times from slowing down. An unstable test in your program occasionally rejects good boards and forces unnecessary rework. Therefore, it is worth spending extra time to stabilize a test.

If your signatures on counters are not stable:

1. Check that your fixture has adequate driver/receiver ground and V_{CC} return wiring.

   Inadequate grounding is the most frequent cause of counter instability.

   For additional information about wiring, refer to the **Z1800-Series Fixturing Guidebook**.
2. Check for possibility of crosstalk between the counter's clock input and any of its outputs.

   If the clock line and outputs are all connected to the same driver/receiver board, move the clock line to a more distant channel and add a separate ground wire in parallel. Twist the new clock lead and ground wire together to couple them electromagnetically. Another possible problem is fast edges of outputs causing reflections. Reflections can clock registers on ripple counters.

3. Check for feed-back paths in the board-under-test which might cause a change in the backdrive state after the clock line should have settled.

   Break up a feedback path with a digital guard. If the same point needs to be guarded for a large number of tests, you can put it in the disable table.

4. Look at the signal with an oscilloscope or logic analyzer.

   Is there a stable region somewhere in the Listen Window even though the signature of the whole pattern is unstable? Can you adjust the Listen Window's From, To and While parameters to exclude the unstable areas?

5. Use an asynchronous signature type (Count or High) instead of a CRC.

   If you can settle on a fairly narrow acceptance band, the test will be stable. If a wide range of Counts is reported, the test probably is not usable.

Test Stability

Clock division will help test stability only when the driver or DUT does not pass through the threshold soon enough to guarantee that the result has propagated to the measurement circuits. Turning on the Terminators may help sometimes, but you should know why it worked and why it will work in all production circumstances. Terminators in the fixture can help reduce signal reflections. In digital tests, you may need to change the clock rate, add or delete guards or disables, or connect terminators.

You should disable free-running clocks on the board-under-test to prevent noise from affecting the test. Spikes from clock signals are capable of causing erratic test results, especially of sequential circuits. If the program generator does not have a template for the clock sources on your board, it cannot add the necessary disabling information. You must identify clock sources and add nodes to the disable table to turn clocks off during testing.

Test stability can change over time as parts from different vendors enter the production line, and vendors change their parts. Your process monitoring procedures should call for examination of in-circuit tests that produce larger-than-average numbers of failure messages.

Check for IC ground noise. If the IC ground is unstable, false tests can occur.

Vector Tests

In addition to the tools used for verifying other tests, the following are useful in verifying vector tests:

- Next, RPT, SOF

  The vector editor includes the keystroke verification tools SOF, Next, Prev, and RPT.

  SOF halts burst execution if a bit or bits fail.

  Next advances the vector editor pointer to the next failing bit.

  RPT causes the vector burst to repeat rapidly.
- Timing and terminators
- Scope synchronization and test points
- Sync pulses and marker bits in the vector Test Properties
- Scrolling pointer and jump scrolling
- Character representations
- Pin records
- Menu modification
- Test configuration menu

- Fault Inject

  Use Fault Inject to test the ability of the vector to detect different faults while you are verifying.

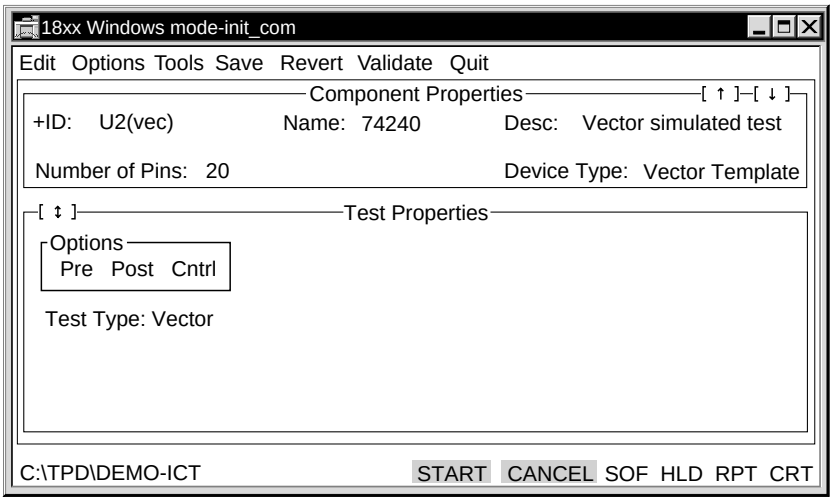
  Refer to the **Z1800-Series Component Test Reference**, Chapter 9, for information on using Fault Inject.

You can open other vector verification tools from a vector test. Since you have not created a vector test in this tutorial, you will view the vector test in the Z1800-series system software's DEMO program.

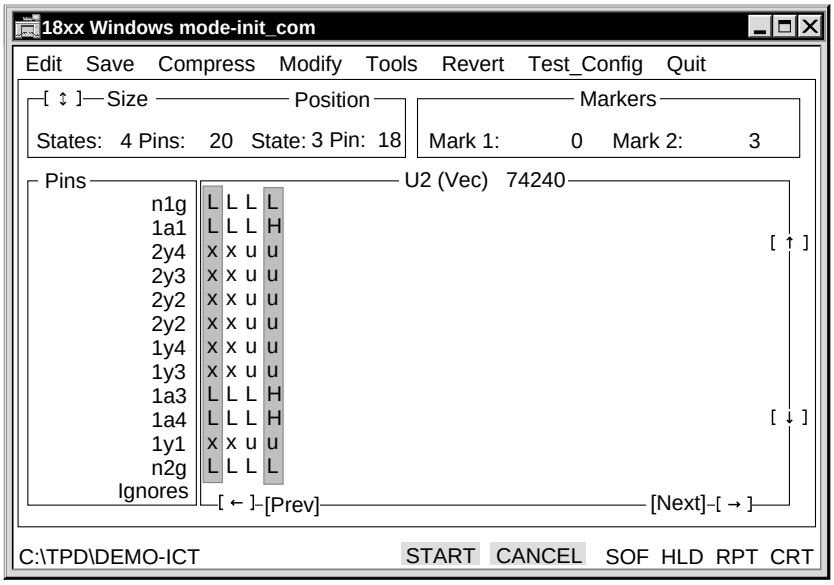
Exercise: View the vector editor window.

1. From the Main menu bar click **Files**.
2. Click **Select**.
3. Click **DEMO** from the C:\TPD window.

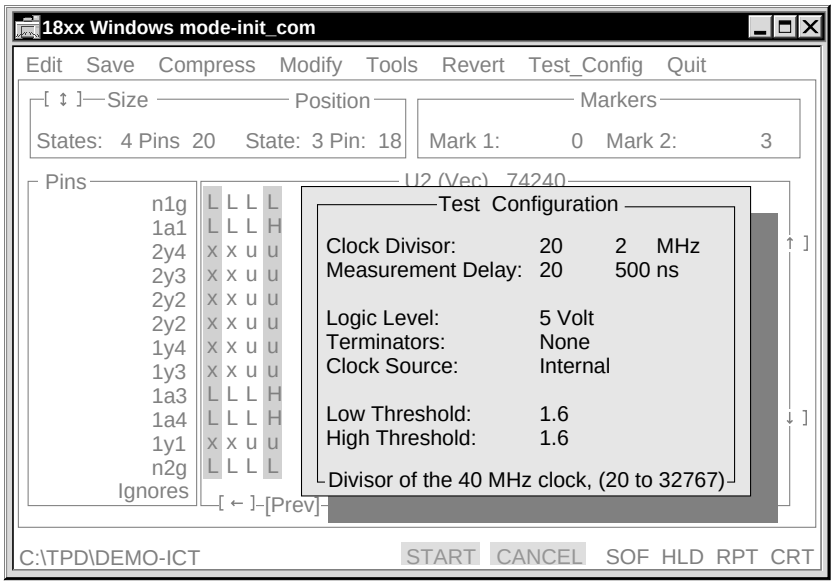
   C:\TPD\DEMO - ICT is on the status bar.
4. From the Main menu bar select **Edit/Digital/Components**.
5. Click **U2(Vec)**, and Component Properties and Test Properties open.



6 Click the arrow in the upper left corner of Test Properties, and the Vector Editor window opens.



7 Click **Test_Config** in the Vector Editor menu bar, and the Test Configuration window opens.



The Test Configuration window shows the current status of the digital test control features Clock Divisor, Measurement Delay, and Terminators.

Clock Divisor

The clock divisor sets the maximum frequency rate that digital patterns can be applied. The internal master clock rate is 40 MHz, so a divisor of 20 yields a pattern application rate (max) of 2 MHz. In a vector test, some patterns may be slower than this if a great number of changes occur on the next pattern in the vector.

Measurement delay

Measurement delay sets the time delay for the measurement strobe relative to the change clock that triggers all pins to change from pattern to pattern. The units are expressed in numbers of 25 ns increments from the change clock, therefore 20 corresponds to 500 nanoseconds, 10 corresponds to 250 ns, and so on.

If a specified measurement delay is longer than the time it takes for a pattern to execute, the measure strobe is truncated by the next change clock and occurs at that time. This usually results in a stable measurement even though it is at the change clock because everything is settled, and the data is latched before the new data propagates.

Terminators

Terminators are used for digital tests. Use the rotating option field to apply resistive loads to all measurements. Terminators are usually required for testing open-collector outputs and for verifying the enable of 3-state devices.

The choices are:

- None
- Pwr5 1K Up
- Pwr5 500 Up
- Pwr5 1K Down
- Pwr5 500 Down
- Pwr5 1K Term
- Pwr5.5 1K Up
- Pwr5.5 500 Up
- Pwr5.5 1K Term.

The pullups are to either

- +5 V
- Programmable 3 V (5.5) supply.

The pulldowns are to ground. The 1K terminator has 1K to +5 V and 1K to ground.

Low Threshold	-2 to +9.95 Volts	Default is 1.6
High Threshold	-2 to +9.95 Volts	Default is 1.6

Logic Level

In the Logic Level field, you can specify 3 volt or 5 volt logic. To return to the tutorial program from the Test Configuration pop-up window:

1. Close the Test Configuration window.
2. Click **Quit** until you return to the Main menu bar.
3. From the Files menu, click **Select**.
4. Click **Tutorial** from the C:\TPD window.

Notes on Verifying Vector Tests

- You can use test jack signals in verifying a vector test.
- The test jack signals, test envelope and listen, are available for use in vector tests.
- Test envelope is active low and stays low anytime the burst is occurring.
- Listen is active high, and it is high only during a subset of the test envelope active time when actual measure states occur.

- You can generate more specialized synchronization and verify signals by adding in another pin in the vector itself, then customizing its high/low pattern to produce the required signal. With this technique, you can generate marker bits, triggers for instrumentation, and so on.
- To move through the vector:

  Use the scroll bars, or click the state and pin fields under the position block of the editor.

  Enter the appropriate coordinates.
- The editor advance to that location. You can move marker bars to any state by dragging or using keyboard-direct-entry commands.

Trailer

The Trailer provides information about termination of the program and passing or failing tests. It can also provide information about program chaining. Through the Valid test step it closes the datalogging process. When verifying your test program, use the Trailer to evaluate system and user flags.

Tutorial References

The following references are in the **Z1800-Series Component Test Reference**, Chapter 3.

- Information on editing the Trailer
- Trailer Message Step

Verifying a Section Test

It is possible that testing a component leaves minute voltage charges on surrounding components that can interfere with subsequent component tests. A possible remedy for this situation is to resequence the components in the section. Running all the tests in a section tells you whether the sequence of tests in the section is workable.

Exercise: Run a section test.

Verify a section of the Z1800-series system software's DEMO program.

1. From the Main menu bar click **Files**.
2. Click **Select**.
3. Click **DEMO**.

   C:\TPD\DEMO - ICT appears in the status bar.
4. From the Main menu bar select **Edit/Passive/Resistors**.
5. At the bottom of the window, click **RPT** to select it.
6. Click **Start** to proceed to the next test.

   Data about the test appears during execution.
7. Continue to click **Start** until all the resistors are tested and the window closes.

In the Demo program, the tests work in their current sequence. If the tests do not work in your program, change the sequence of components until the test runs reliably.

1. Click **Quit** until you return to the Main menu bar.
2. Select **Files/Select**.
3. Click **Tutorial**.

Verification Using Run Mode

When all the tests are working individually, check program execution from the production operator's perspective. Run the program with Allprint on so you can view the failure messages. Check for stability with one board, then with many boards.

Using Allprint to View Failure Message

When Allprint is on, a failure prints for all tests whether they pass or fail. You have the option of printing a message if a test fails.

To turn Allprint on:

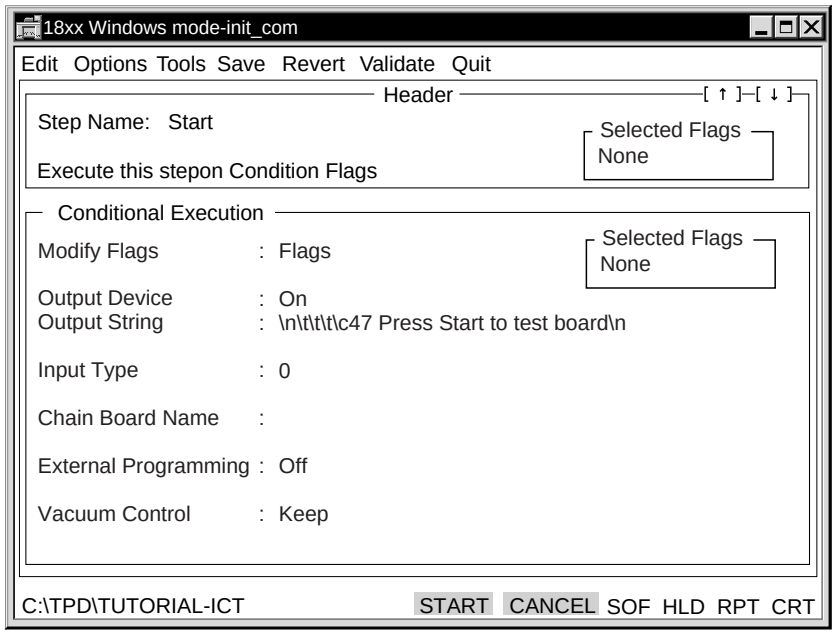
1. Select **Files/Edit/Header/PRGMVARS**.
2. Click **Report Variables**
3. Click the **Allprint** field to ON.

   When prompted, click **Yes** to change your edit.
4. Click **Quit** to return to the Main menu bar.

Check Test Stability With One Board

To check stability with only one board:

1. Select **Files/Edit/Header/PRGMVARS**.
2. Click the page down arrow in the upper right corner of the Header window until you reach the page with Step Name: Start.



3. Click the **Input Type** field to None.

   The board test normally stops at its end so an operator can change the board-under-test. Selecting None removes the stop at the end of the test, so the test runs continuously.
4. From the menu bar, click **Quit**.
5. At the Save prompt, click **Yes**.
6. Click **Quit** until you return to the Main menu bar.
7. Click **Run** from the Main menu bar.

   As the program runs continuously, observe whether the program shows any intermittent behavior.
8. Press **F10** to stop the program.

You can check test stability by running your program with a large number of production boards. Observe the failure messages to ensure that they result from failures, not from excessively tight limits or unstable test steps.

Notes on Verifying the Program

As the test runs, messages show the test's progress. Determine the following:

- Is there enough vacuum-on delay.

  If there is not enough vacuum-on delay, increase the delay in Header/PRGMVARS.
- Will the CRT messages and interventions (adjustment steps, for instance) make sense to the production operator?

  If not, change the messages.
- How long does the program take to run?
- Did any tests fail?

  Verify the tests that failed.
- Are the failure messages formatted properly?

  If not, reformat them to suit your test environment.

Final Checks

The following is a list of the last things to check to make sure your test program runs smoothly:

- Check the Parts List

  Compare the board's parts list against the Allprint output for parts not tested. This information will help plan the functional test stages that may be required after the in-circuit test. In most cases, a functional test will diagnose only those faults not diagnosed during the in-circuit phase.
- Restore Variables

  Edit the PRGMVARS test step to restore the variables you changed for verification purposes. Pay attention to Section Abort. Although Section Abort can be turned off when verifying a good board, there is potential board damage when executing a test with Section Abort off.

  Click **Off** in PRGMVARS/Status Display to speed test execution.
- Correct Component Database Files

  Correct the component database to account for components added or deleted during verification. Correcting the component database files ensures that the component database, IPL.DBF, agrees with your test program, ICT.TST.

  Refer to the **Z1800-Series Component Test Reference**, Chapter 7, for more information about correcting component database files.
- Documentation for Repair

  To provide documentation for the repair technician, make a Nodes-to-Components list and a Components-to-Nodes list.

  1. From the Main menu bar, select **Pgen/Reports**.
  2. Click **Node List**.
  3. Click **Yes** to update the IPL database.
  4. Click **Component List**.
  5. Click **Quit** to return to the Main menu bar.

This completes the tutorial.

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